

V08TC065A1X11

650V GaN Power Switch

Preliminary Datasheet



Description

The D³GaN (Direct Drive D-Mode) V08TC065A1X11 Power Switch integrates a patented, high-density, lateral GaN power transistor, into a **Normally - Off** product with low $R_{DS(on)}$ and exceptionally efficient switching performance.

An **Isolated High Power SMD** package enables applications requiring High Power and Efficiency, with Low Volume and Cost.

The integrated safety function ensures safe operation during system start up and shutdown, while having no impact on the switching performance of the GaN transistor.

Key features

- Ultra-fast switching
- Kelvin connection
- Normally-Off
- Ultra low $R_{DS(on)}$ of 8m Ω
- Fully isolated package (3.5KV)
- High Threshold Voltage >5V
- Driven by standard 15V driver
- Top cooling package

Applications

- Automotive
- AC motors
- AC-DC Power Supply
- Battery chargers
- Laser driver

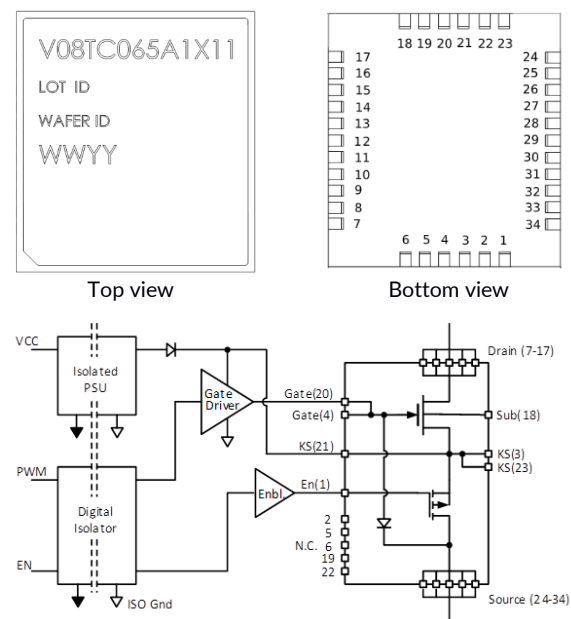


Figure 1 - Package Pinout & Simplified application scheme

Key Performance Parameters

Parameter	Value	Units
V_{DS}	650	V
$R_{DS(on)}$	8	m Ω
Q_G	200	nC
I_D	200	A

Pin	Function
24-34	Source
7-17	Drain
4, 20	GaN Gate ¹⁾
3, 21, 23	Kelvin Source ¹⁾
1	Enable (PMOS Gate)
18	GaN Substrate
2, 5, 6, 19, 22	NC ²⁾

1) Only connect one Gate and one Kelvin pins

2) Do not connect

Ordering Information:

Part Number	Packing	Marking	Ordering Number
V08TC065A1X11	Tray	V08TC065A1X11	V08TC065A1X11T

Maximum ratings (Tc =25°C unless otherwise specified)					
Parameter	Symbol	Min	Max	Unit	Conditions
Drain-Source breakdown voltage	$V_{(BR)DS}$	650	-	-	
Drain Source Transient voltage	$V_{DS(transient)}$		800	V	Pulse $\leq 1\mu s$
Continuous Drain current ³⁾	I_D	-	200	A	$T_C = 100^\circ C^{1)}$
			170		
Gate Source voltage	V_{GS}	-20	0	V	Pin4, 20 to pin2, 23
Transient Gate Source voltage	$V_{GS(transient)}$	-25	6	V	Pulse $\leq 1\mu s$
Power dissipation	P_{TOT}	-	500	W	
Operating and storage temperature	T_j, T_{stg}	-55	+150	$^\circ C$	
Continuous reverse current	I_s	-	200	A	$T_C = 25^\circ C^{1)}$
Reverse pulse current ¹⁾	$I_{s,pulse}$	-	300	A	
Gate leakage	I_{gss}	-	200	μA	$V_{DS} = 650V,$ $V_{GS} = -15V$
Thermal Characteristics					
Thermal resistance, junction-case	$R_{\theta JC}$	-	0.1	$^\circ C/W$	
Thermal resistance, junction - ambient	$R_{\theta JA}$	-	65	$^\circ C/W$	
Soldering peak body temperature	T_p	-	260	$^\circ C$	
Time within 5°C from peak soldering temperature	t_c	-	30	S	

3) Limited by Tj max of 150°C, Vgs = 0V, considering Rth(JC) in a discrete package = 0.1°C/W. Limited by die interconnect.

4) Duty cycle =10% and pulse width limited by Tjmax. Limited by die interconnect.

Electrical characteristics (T _J =25°C, V _{GS} = -15V unless otherwise specified)						
Parameter	Symbol	Min	Typical	Max	Unit	Conditions
Static						
GaN Gate threshold voltage	V _{th}	-10	-9.5	-9	V	I _D =47mA, V _{DS} =10V
Recommended driving voltage ⁵⁾	V _{DD}	15			V	Refer to driver GND
Threshold voltage ⁶⁾ ref. to driver GND	V _{thGND}	5	5.5	6		V _{DD} =15V
Drain Source leakage current	I _{DSS}	-	3	5	μA	V _{DS} = 650V
		-	75	200		V _{DS} = 650V T _J =150°C
Gate resistance	R _G	-	0.5	-	Ω	f=1Mhz
Drain-Source on state resistance	R _{DS(ON)}	-	8	12	mΩ	V _{GS} =0V I _D =35A
		-	17.5	-		V _{GS} =0V I _D =35A T _J =150°C
GaN Reverse voltage drop- OFF State	V _R	-	-	7.5	V	I _D =10A
		-	-	9.5		I _D =10A T _J =150°C
GaN Reverse voltage drop- ON State	V _R	-	0.08	-	V	I _D =10A, V _{GS} =0V
		-	0.17	-		I _D =10A, T _J =150°C V _{GS} =0V
Reverse recovery time	t _{rr}	-	-	0	ns	
Reverse recovery charge	Q _{rr}	-	-	0	nC	
Output Charge	Q _{oss}	-	-	360	nC	V _{DS} =400V
Dynamic						
Input capacitance	C _{iss}	-	1900	-	pF	f=1MHz V _{DS} =400V
Output capacitance	C _{oss}	-	500	-		
Reverse transfer capacitance	C _{rss}	-	70	-		
Effective Output Capacitance, Energy Related	C _{O(ER)}	-	-	1100	pF	V _{DS} = 0-400V
Turn-on delay time	t _{d(on)}	-	13.5	-	ns	V _{DS} =400V, V _{DD} =15V ¹ I _D =35A, BJT Gate Buffer R _{base} = 100Ω for ON & 20Ω for OFF
Fall time	t _f	-	22	-		
Turn-off delay time	t _{d(off)}	-	8.1	-		
Rise time	t _r	-	10.5	-		

5) In operation GaN V_{gs} swings from -V_{DD} (OFF state) to 0V (ON state).

6) Refers to driver GND, see simplified application scheme. Threshold voltage defined as V_{th}= V_{DD}+V_{th-GaN}= 15V+(-9)V=6V

Electrical characteristics ($T_J = 25^\circ\text{C}$ unless otherwise specified)						
Parameter	Symbol	Min	Typical	Max	Unit	Conditions
Gate Charge characteristics						
Gate to Source charge	Q_{GS}	-	8	-	nC	$V_{GS}=0\text{V to }-14\text{V}$ $V_{DS}=400\text{V } I_D=32\text{A}$
Gate to Drain charge	Q_{GD}	-	130	-		
Total Gate charge	Q_G	-	200	-		

Enable Pin Characteristics						
Parameter	Symbol	Min	Typical	Max	Unit	Conditions
PMOS V_{th}	$V_{th-PMOS}$	-3		-2	V	Pin 1 referenced to Pins 3,21,23
Absolute maximum rating	V_{En-KS}	-20	-	10		

Recommended Operational Voltages						
Parameter	Symbol	Min	Typical	Max	Unit	Conditions
Pin 1, Enable signal referenced to ISO GND						
Recommended V_{DD} voltage for PMOS Enable	$V_{En-PMOS}$		13.5		V	For 15V V_{DD}
Recommended V_{DD} voltage for PWM UVLO	$V_{PWM-UVLO}$		14			

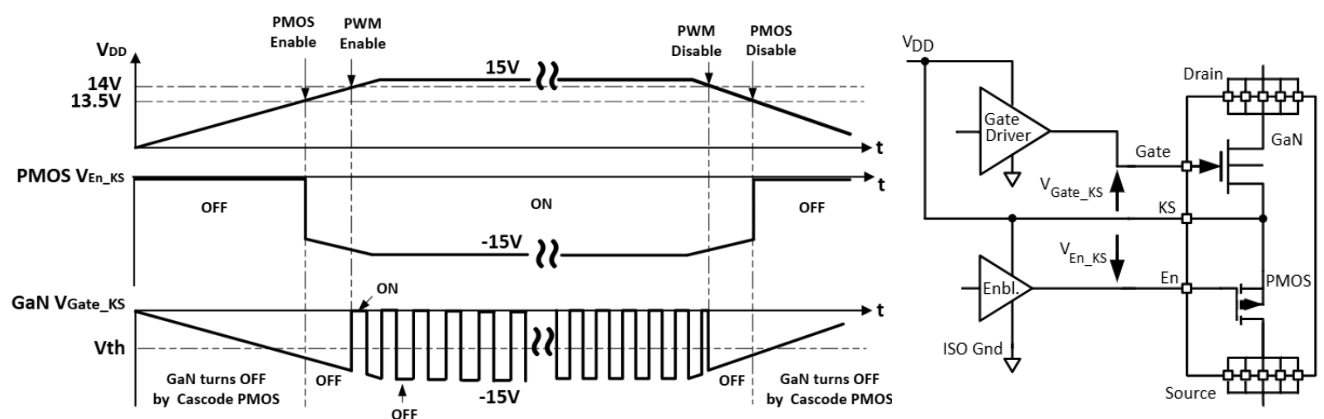


Figure 2 – Simplified D3GaN safe operation voltage references for Enable & PWM UVLO

Typical Characteristics at 25C° (unless noted otherwise)

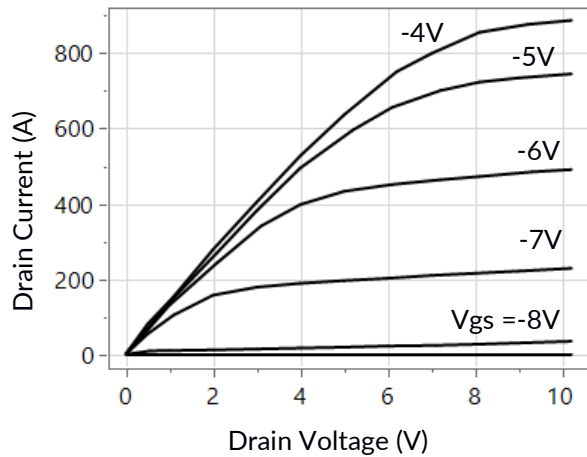


Figure 3 - Output (Forward) Characteristics

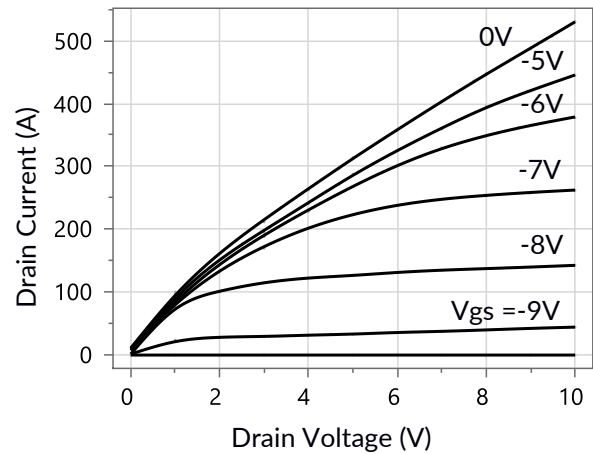


Figure 4 - Output (Forward) Characteristics Tj=150C

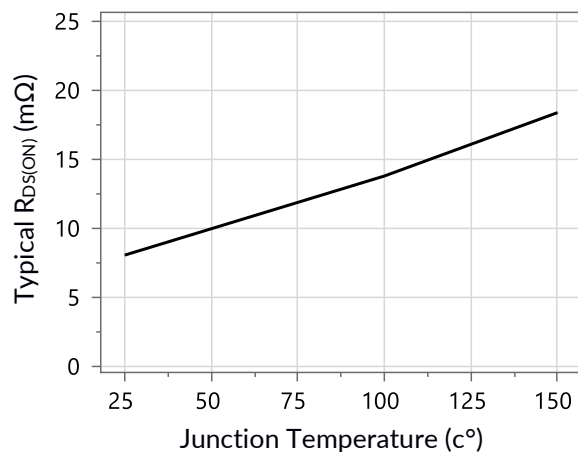


Figure 5 - ON-State Resistance vs. Temperature

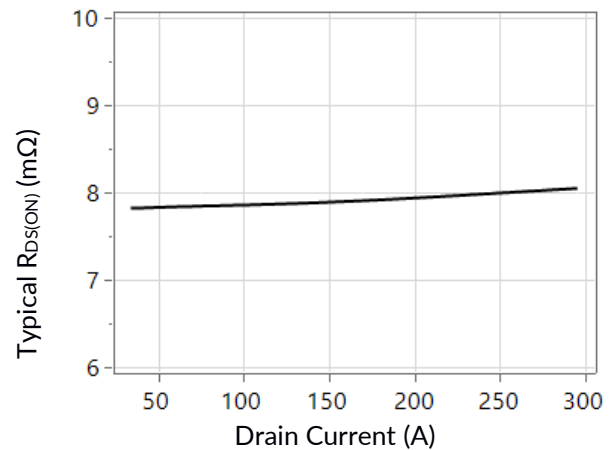


Figure 6 - ON-State Resistance vs. Current at 25°C

Typical Characteristics cont.

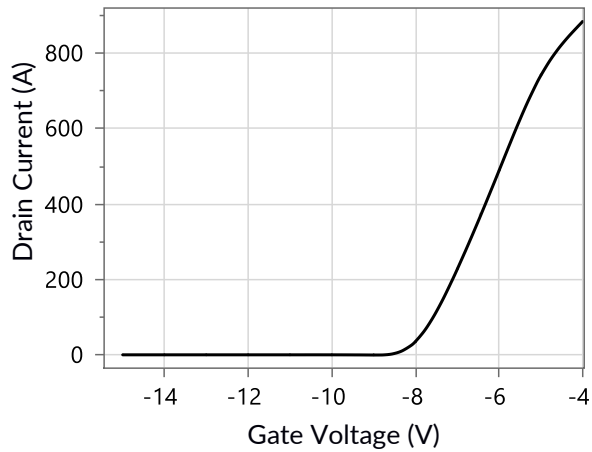


Figure 7 - Transfer Characteristics

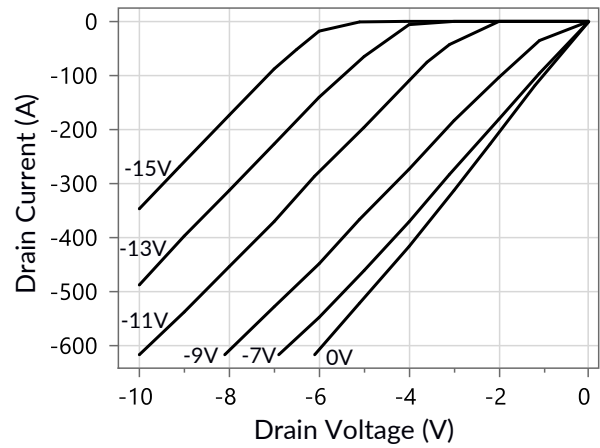


Figure 8 - Reverse Conduction vs. Gate Voltage

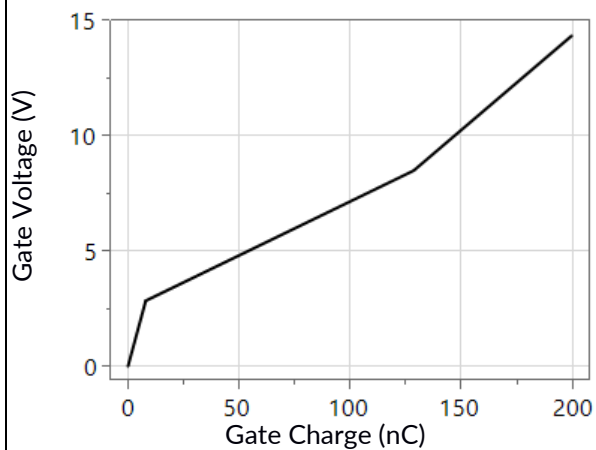


Figure 9 - Gate Charge

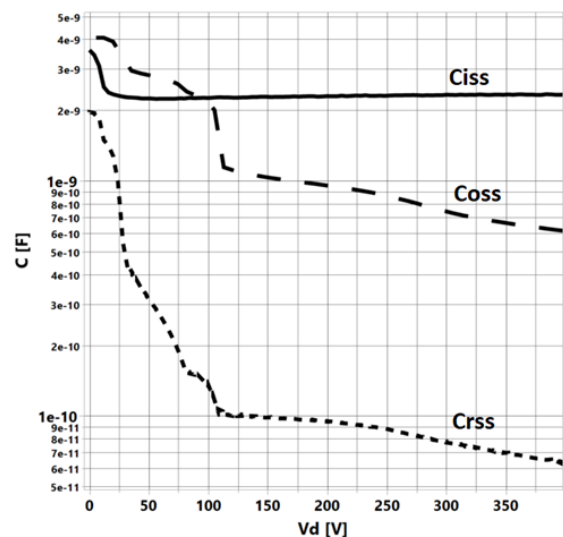


Figure 10 Typical Capacitance

Typical Characteristics cont.

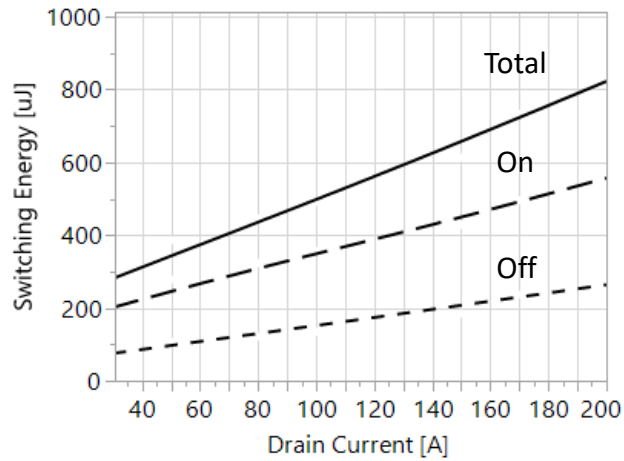


Figure 11 - Typical Switching Energy vs Drain Current

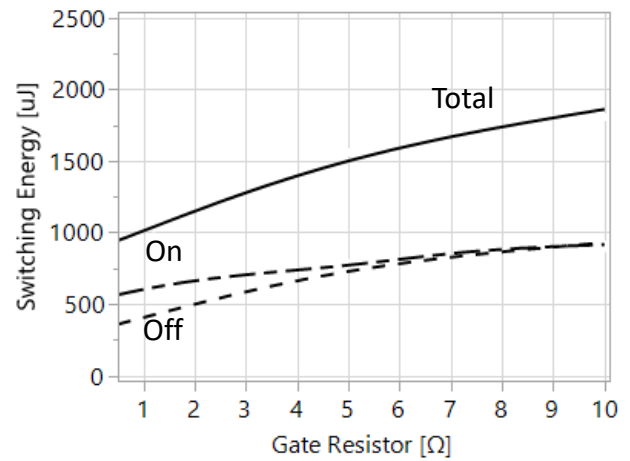


Figure 12 - Typical Switching Energy vs Gate Resistor

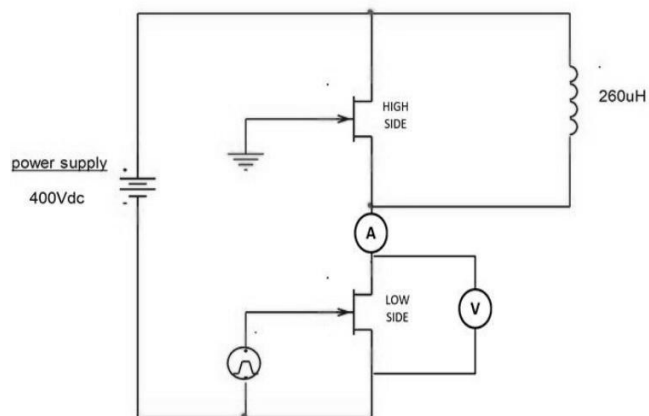


Figure 13 - Switching parameters test circuit

Switching Time Waveforms

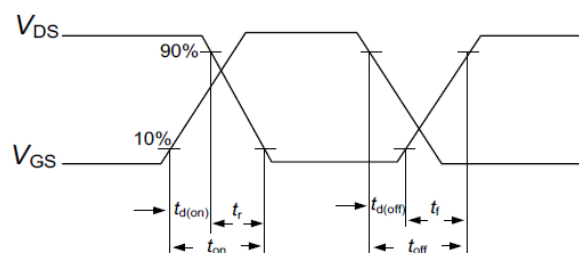


Figure 14 - Switching time waveforms

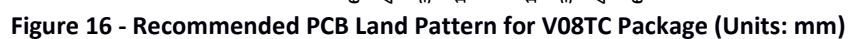
Figure 1: Dimensions of the V08TC065A1X11 package. The figure consists of three views: a top view, a side view, and a pin 1 corner detail.

Top View: The package is square with overall dimensions of 21.79 mm by 19.81 mm. The top view shows the package marking: "V08TC065A1X11", "LOT ID", "WAFER ID", and "WWYY". The "LOT ID" is located at the top left, "WAFER ID" is below it, and "WWYY" is below that. The "PIN #1" is indicated at the bottom left corner.

Side View: The package height is 3.40 mm. The "Seating Plane" is indicated at the bottom. The package is shown in a cross-section view.

PIN #1 Corner Detail: This view shows the corner of the package where the pins are located. The pins are numbered 1 through 34. The dimensions for the pin spacing and the corner location are provided. The "PIN #1 Corner" is indicated at the bottom right.

Recommended Land Pattern:



Rev.	Date	Content of Change	Owner
1	31/07/2023	New datasheet and template under new part number	I.B
2	22/08/2023	Changed Rdson value slightly based on updated die measurements, revised Pin characteristics table.	I.B
3	16/10/2025	Product changed according to PCN 2025-001	I.B
4	21/04/2026	Updated graphs	I.B

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