

# V22TG065S1X04

## 650V D<sup>3</sup>GaN™ Power Switch

### Preliminary Datasheet



### Description

The D<sup>3</sup>GaN (**D**irect **D**rive **D**-Mode) V22TG065S1X04 Power Switch integrates a patented, high-density, lateral GaN power transistor, into a **Normally - Off** product with low  $R_{DS(ON)}$  and exceptionally efficient switching performance. The D<sup>3</sup>GaN technology has been implemented into an **Isolated High-Power SMD** package - it is very effective in applications requiring High Power and Efficiency, with Low Volume and Cost. The integrated safety function ensure safe operation during system start up and shutdown, while having no impact on the switching performance of the GaN transistor.

### Key features

- Ultra-fast Switching
- Kelvin Source connection
- Depletion Mode GaN in Normally-Off package
- Top cooling fully isolated package (3.5KV)
- No Reverse-Recovery charge
- low On State resistance of 22mΩ
- Low Gate Charge
- High noise immunity with  $V_{th} > 5V$
- Driven by standard 15V Si-MOSFET driver

### Applications

- Solar Inverter
- AC-DC Power Supply
- AC motors
- Battery chargers
- Automotive
- Laser driver

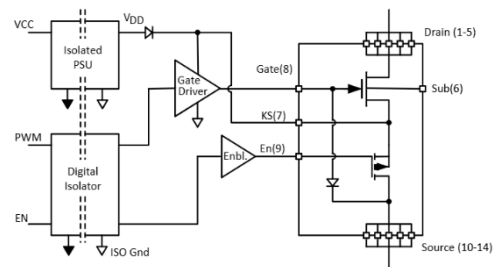


Figure 1 - Package Pinout & Simplified application scheme

### Key Performance Parameters

| Parameter     | Value | Units |
|---------------|-------|-------|
| $V_{DS}$      | 650   | V     |
| $R_{DS(ON)}$  | 22    | mΩ    |
| $Q_G$         | 41    | nC    |
| $I_{D,pulse}$ | 280   | A     |
| $I_D$         | 80    | A     |

| Pin   | Function      |
|-------|---------------|
| 1-5   | Drain         |
| 6     | Substrate     |
| 7     | Kelvin Source |
| 8     | Gate          |
| 9     | Enable        |
| 10-14 | Source        |

### Ordering Information:

| Part Number   | Packing | Marking       | Ordering Number |
|---------------|---------|---------------|-----------------|
| V22TG065S1X04 | Tray    | V22TG065S1X04 | V22TG065S1X04T  |

| Maximum ratings (Tc =25°C unless otherwise specified) |                     |     |      |         |                             |
|---|---------------------|-----|------|---------|-----------------------------|
| Parameter   | Symbol              | Min | Max  | Unit    | Conditions                  |
| Drain-Source breakdown voltage                        | $V_{(BR)DS}$        | 650 | -    | -       |                             |
| Drain Source Transient voltage                        | $V_{DS(transient)}$ |     | 800  | V       | Pulse $\leq 1\mu s$         |
| Continuous Drain current                              | $I_D$               | -   | 80   | A       | $T_C = 100^\circ C$         |
|   |                     |     | 62   |         |                             |
| Pulsed Drain current <sup>1)</sup>                    | $I_{D,pulse}$       | -   | 150  | A       |                             |
| Gate Source voltage                                   | $V_{GS}$            | -20 | 0    | V       |                             |
| Power dissipation                                     | $P_{TOT}$           | -   | 278  | W       |                             |
| Operating and storage temperature                     | $T_j, T_{stg}$      | -55 | +150 | °C      |                             |
|   | $T_C$               |     | +150 |         |                             |
| Continuous reverse current                            | $I_s$               | -   | 80   | A       |                             |
| Reverse pulse current <sup>1)</sup>                   | $I_{s,pulse}$       | -   | 150  | A       |                             |
| Gate leakage <sup>2)</sup>                            | $I_{gss}$           | -   | 200  | $\mu A$ | See Note 2                  |
| Thermal Characteristics                               |                     |     |      |         |                             |
| Thermal resistance, junction-case                     | $R_{\theta JC}$     | -   | 0.3  | °C/W    | Junction to top thermal pad |
| Thermal resistance, junction - ambient                | $R_{\theta JA}$     | -   | 65   | °C/W    |                             |
| Soldering peak body temperature                       | $T_p$               | -   | 260  | °C      |                             |
| Time within 5°C from peak soldering temperature       | $t_c$               | -   | 30   | S       |                             |

- 1) Duty cycle =10% and pulse width limited by  $T_{jmax}$ .
- 2) High Gate leakage is attributed to D1 reverse leakage at 150C.



| Electrical characteristics ( $T_J = 25^\circ\text{C}$ , $V_{GS} = -15\text{V}$ unless otherwise specified) |                            |     |         |      |                  |  |
|--|----------------------------|-----|---------|------|------------------|--|
| Parameter  | Symbol                     | Min | Typical | Max  | Unit             | Conditions   |
| GaN Gate threshold voltage <sup>3)</sup>   | $V_{th}$                   | -10 | -9      | -8   | V                | $I_D=1\text{mA}$   |
| Threshold voltage <sup>4)</sup> ref. to driver GND   | $V_{th-VDD}$               | 5   | 6       | 7    | V                | $I_D=1\text{mA}$ $V_{DD}=15\text{V}$   |
| Recommended driving voltage  | $V_{dd}$                   | 0   | -       | 15   | V                | Ref. to driver GND   |
| Transient Gate Source voltage <sup>5)</sup>  | $V_{GS(\text{transient})}$ | -25 | -       | +6   | V                |  |
| Drain Source leakage current   | $I_{DSS}$                  | -   | 3       | 4    | $\mu\text{A}$    | $V_{DS}=650\text{V}$   |
|  |                            | -   | 27      | 200  |                  | $V_{DS}=650\text{V}$ $T_J=150^\circ\text{C}$                                 |
| Gate resistance  | $R_G$                      | -   | 1.4     | -    | $\Omega$         | $f=1\text{Mhz}$  |
| Drain-Source on state resistance   | $R_{DS(\text{ON})}$        | -   | 22      | 27   | $\text{m}\Omega$ | $V_{GS}=0\text{V}$ $I_D=35\text{A}$  |
|  |                            | -   | 42      | 52   |                  | $V_{GS}=0\text{V}$ $I_D=35\text{A}$<br>$T_j=150^\circ\text{C}$               |
| Reverse voltage drop-<br>GaN non conductive  | $V_R$                      | -   | -       | 7.5  | V                | $I_D=10\text{A}$   |
|  |                            | -   | -       | 9.5  |                  | $I_D=10\text{A}$ $T_j=150^\circ\text{C}$                                     |
| Reverse voltage drop-<br>GaN conductive  | $V_R$                      | -   | -       | 0.22 | V                | $I_D=10\text{A}$   |
|  |                            | -   | -       | 0.42 |                  | $I_D=10\text{A}$ $T_j=150^\circ\text{C}$                                     |
| Reverse recovery time  | $t_{rr}$                   | -   | -       | 0    | ns               |  |
| Reverse recovery charge  | $Q_{rr}$                   | -   | -       | 0    | nC               |  |
| Output Charge  | $Q_{oss}$                  | -   | -       | 171  | nC               | $V_{DS}=400\text{V}$   |
| Input capacitance  | $C_{iss}$                  | -   | 780     | 820  | $\text{pF}$      | $f=1\text{MHz}$<br>$V_{DS}=400\text{V}$                                      |
| Output capacitance   | $C_{oss}$                  | -   | 200     | 240  |                  |  |
| Reverse Transfer capacitance   | $C_{rss}$                  | -   | 26      | 30   |                  |  |
| Effective Output capacitance,<br>Energy Related  | $C_{O(\text{ER})}$         | -   | -       | 278  | $\text{pF}$      | $V_{DS}=0-400\text{V}$   |
| Turn-On delay time   | $t_{d(\text{on})}$         | -   | 12      | -    | ns               | $V_{DS}=400\text{V}$ $V_{DD}=15\text{V}$<br>$I_D=35$ $R_{gate}=1\text{ Ohm}$ |
| Fall time  | $t_f$                      | -   | 8.6     | -    |                  |  |
| Turn-Off delay time  | $t_{d(\text{off})}$        | -   | 15.5    | -    |                  |  |
| Rise time  | $t_r$                      | -   | 8.8     | -    |                  |  |

3) After applying Enable signal, see operation circuit below.

4) In operation  $V_{gs}$  swings from  $-V_{DD}$  (OFF state) to  $0\text{V}$  (ON state).  $V_{th-VDD}$  threshold voltage is defined as  $V_{DD} + V_{th} = 15\text{V} + [-8\text{V}] = 7\text{V}$ .

5) In on/off-state, spike; spike duration  $<1\mu\text{s}$ .

| Electrical characteristics (T <sub>J</sub> =25°C, V <sub>GS</sub> = -15V unless otherwise specified) |                 |     |         |     |      |   |
|--|-----------------|-----|---------|-----|------|---|
| Parameter  | Symbol          | Min | Typical | Max | Unit | Conditions  |
| <b>Gate Charge characteristics</b>   |                 |     |         |     |      |   |
| Gate to Source charge <sup>6)</sup>  | Q <sub>GS</sub> | -   | 4.3     | -   | nC   | V <sub>GS</sub> = 0V to -10V<br>V <sub>DS</sub> =400V I <sub>D</sub> =30A |
| Gate to Drain charge <sup>6)</sup>   | Q <sub>GD</sub> | -   | 33      | -   |      |   |
| Total Gate charge <sup>1)</sup>  | Q <sub>G</sub>  | -   | 41      | -   |      |   |
| <b>Case to Drain Capacitance</b>   |                 |     |         |     |      |   |
| Capacitance  | C <sub>c</sub>  | -   | 20      | -   | pF   | f=1 MHz 0.1V RMS  |

6) After applying Enable signal, see Typical Operation circuit below.

| Enable Pin Characteristics |                      |     |         |     |      |                     |
|----------------------------|----------------------|-----|---------|-----|------|---------------------|
| Parameter                  | Symbol               | Min | Typical | Max | Unit | Conditions          |
| PMOS V <sub>th</sub>       | V <sub>th-PMOS</sub> | -3  |         | -2  | V    | Pin 9 ref. to Pin 7 |
| Absolute maximum rating    | V <sub>En-KS</sub>   | -20 | -       | 10  |      |                     |

| Recommended Operational Voltages                    |                       |     |         |     |      |                         |
|---|-----------------------|-----|---------|-----|------|-------------------------|
| Parameter   | Symbol                | Min | Typical | Max | Unit | Conditions              |
| <b>Pin 9, Enable signal referenced to ISO GND</b>   |                       |     |         |     |      |                         |
| Recommended V <sub>DD</sub> voltage for PMOS Enable | V <sub>En-PMOS</sub>  |     | 13.5    |     | V    | For 15V V <sub>DD</sub> |
| Recommended V <sub>DD</sub> voltage for PWM UVLO    | V <sub>PWM-UVLO</sub> |     | 14      |     |      |                         |

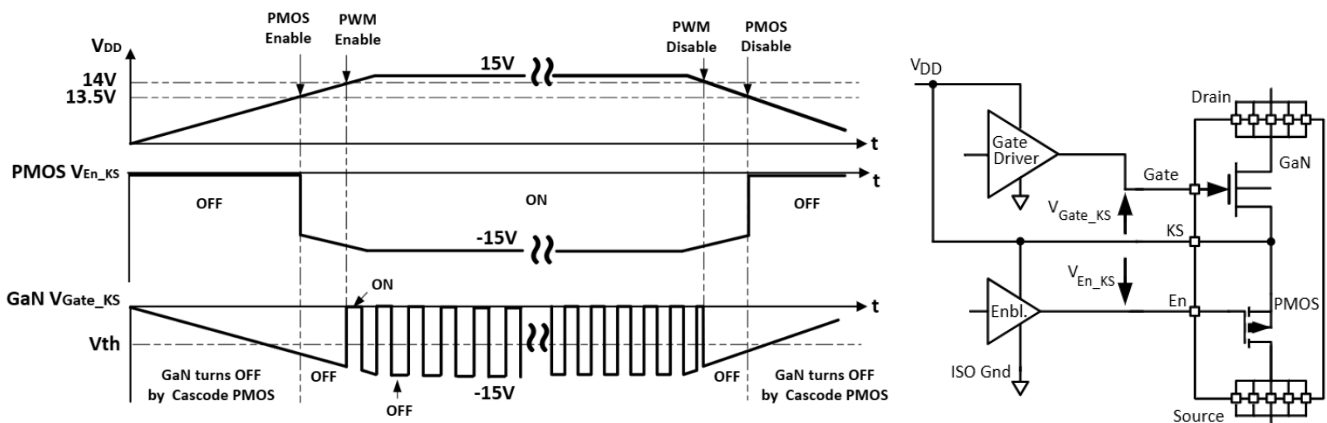


Figure 2 - Simplified D3GaN safe operation voltage references for Enable & PWM UVLO

Typical Characteristics at 25C° (unless noted otherwise)

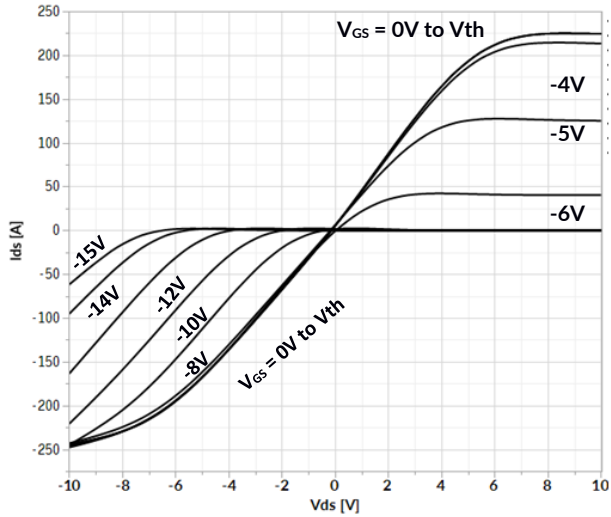


Figure 3 - Output Characteristics

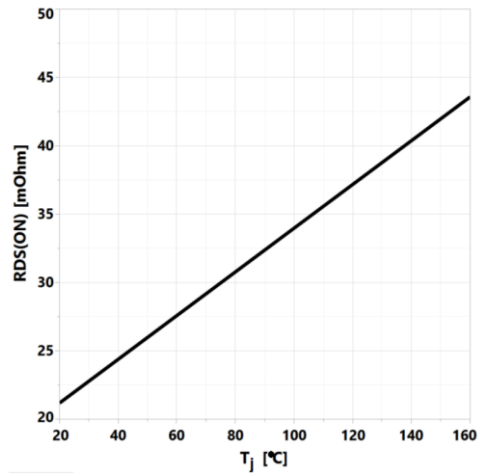


Figure 4 - ON-State Resistance vs. Temperature

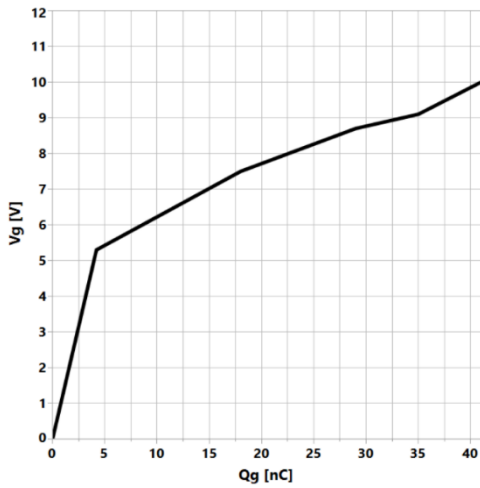


Figure 5 - Typical Gate Charge

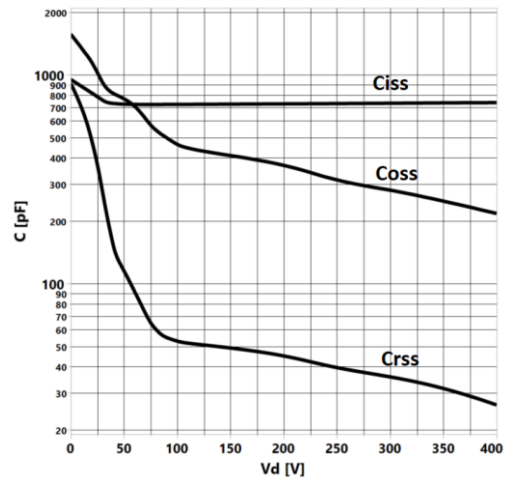


Figure 6 - Typical Capacitances



Typical Characteristics at 25C° (unless noted otherwise)

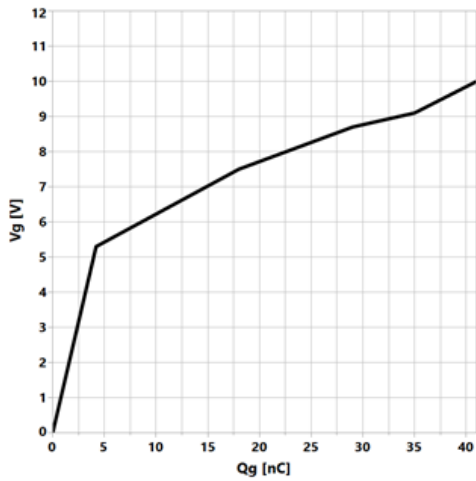


Figure 7 - Gate Charge

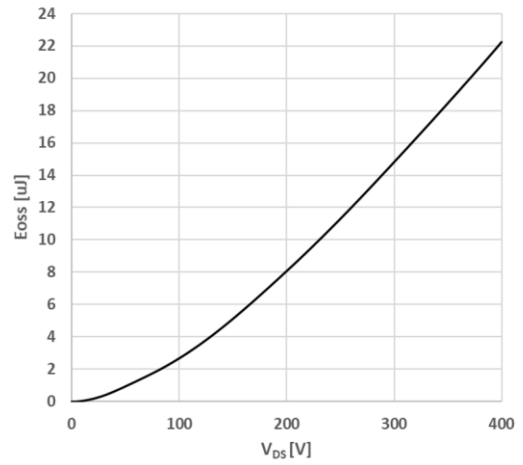


Figure 8 - Typical Coss stored Energy

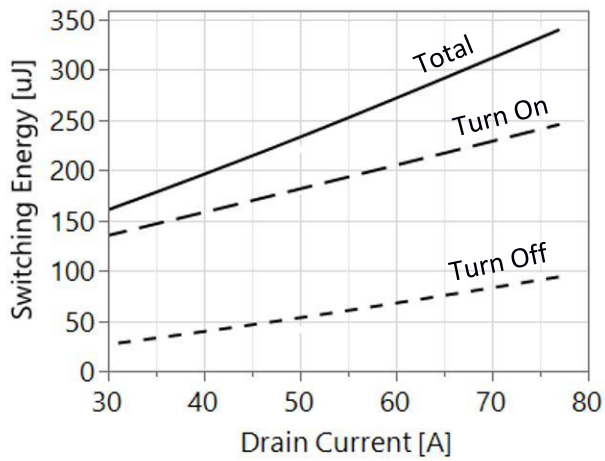
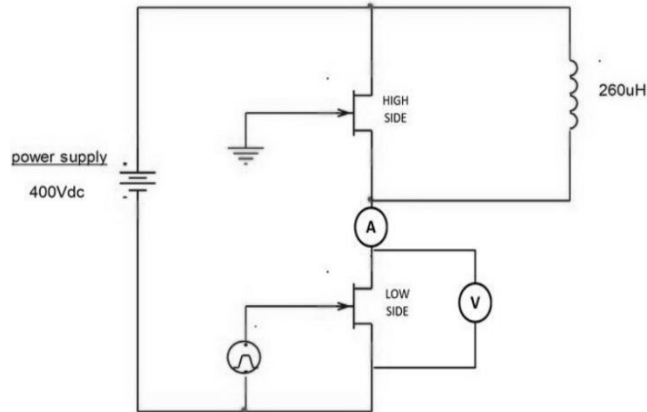


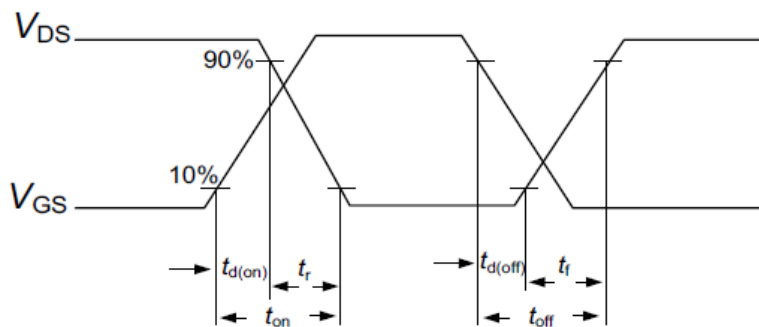
Figure 9 - Typical Switching Energy vs Drain Current at 400V



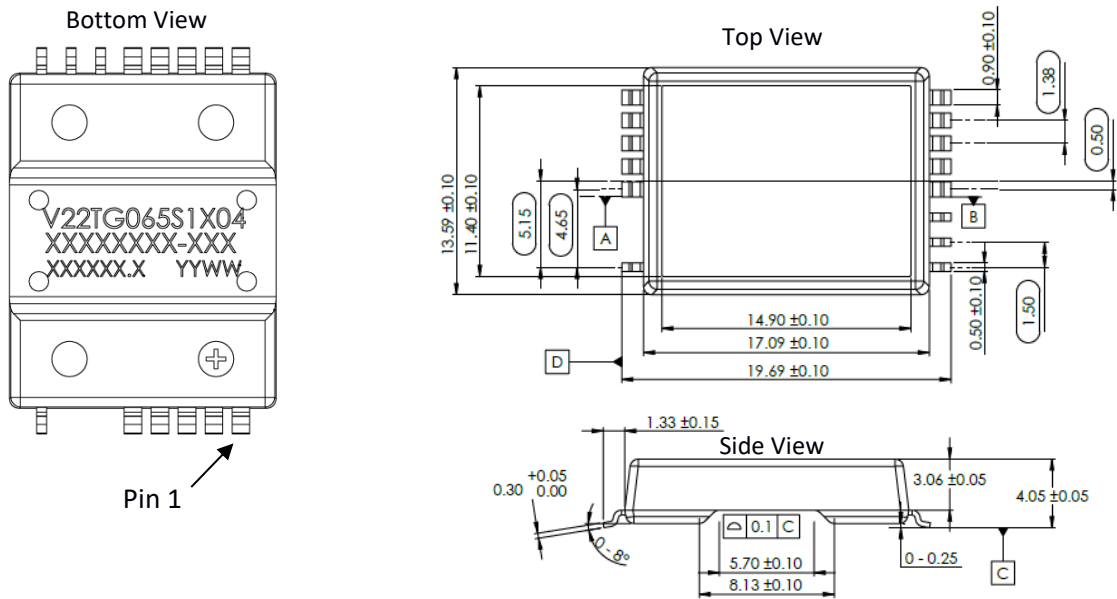
**Test Circuit Schematic:**



**Switching Time Waveforms:**



**Package Outlines:**



**Recommended PCB Land Pattern:**

**RECOMMENDED  
 LAND PATTERN**  
 (units in mm)

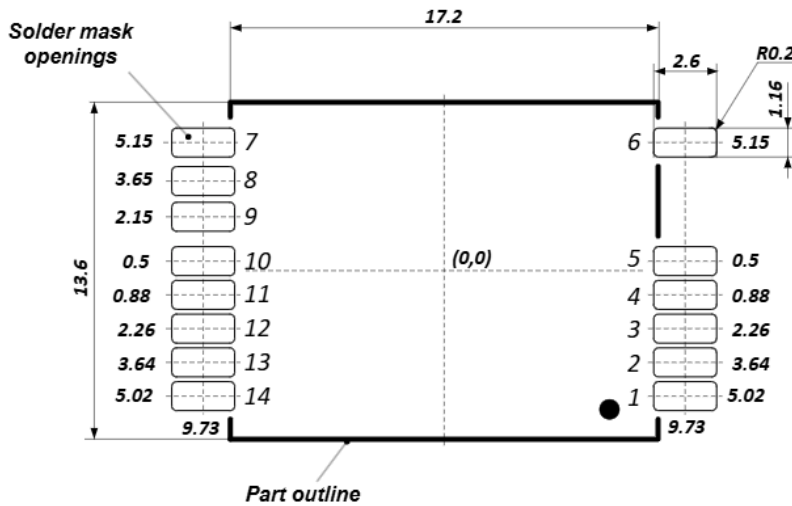


Figure 10 - Recommended PCB Land Pattern for V22TG Package (Units: mm)

# V22TG065S1X04

## Preliminary Datasheet



| Rev. | Date       | Content of Change                                | Owner |
|------|------------|--|-------|
| 1.0  | 26/05/2026 | New datasheet and template under new part number | I.B   |
|      |            |  |       |
|      |            |  |       |

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