GaN FOR EV POWER TRAIN: BREAKTHROUGHS AND CHALLENGES

Yana Ashkinazer, Adam Briga, Gregory Bunin, Ilia Bunin, Joey Chang, Ian Chen, Oren Cohen, Oleg Dubinsky, Alex Firtel, Yuri Gitelmakher, Oded Granot, Nissim Iskhakbaev, Dieter Liesabeths, Michael Manelis, Dima Novo, David Ptashnikov, Yulia Roiter, Memo Romero, Evgeny Rozanov, David Shapiro, Lev Stessin, Ray Tsai, Dana Verpinsky, Valery Verpinsky, Gleb Vetakh, Roman Volkov, Simon Wainwright, Shahar Wagner

and others

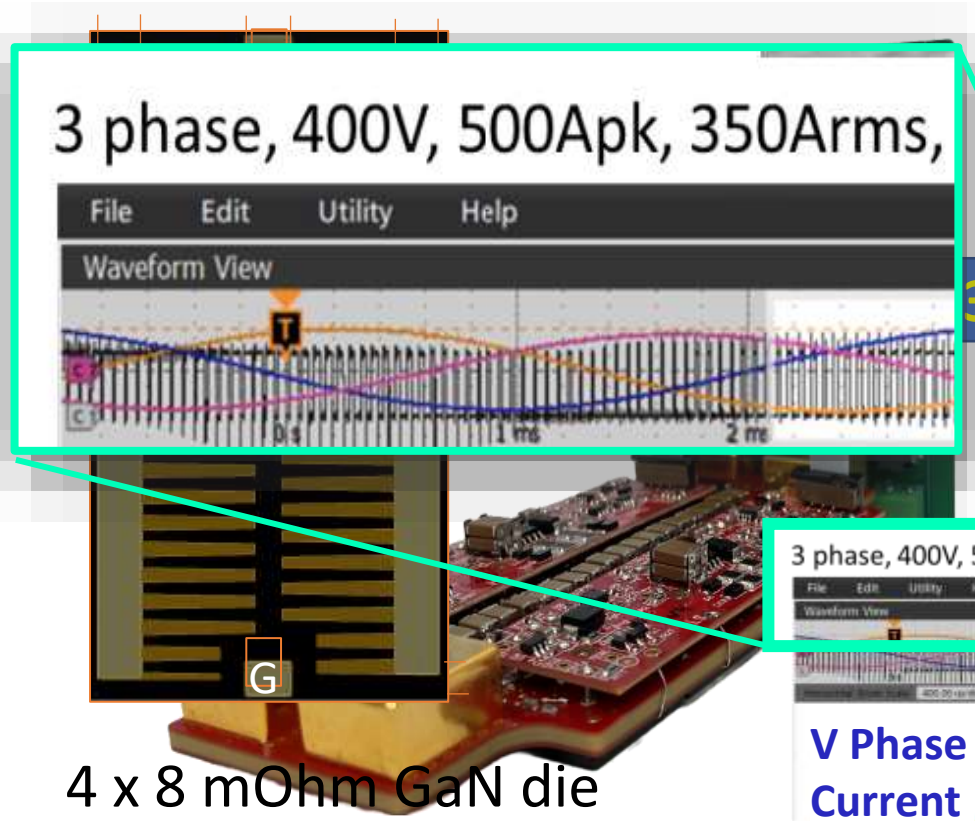
VisIC Technologies

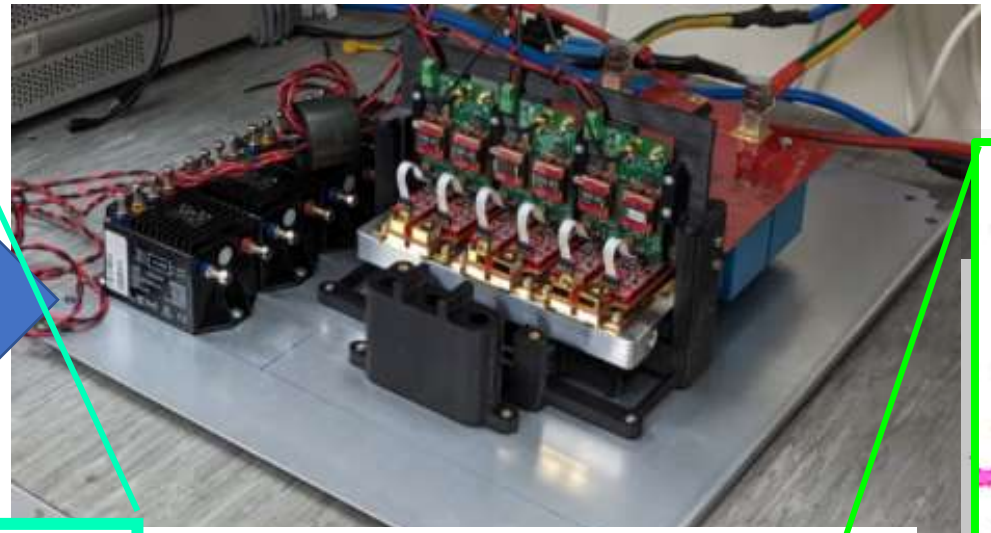
OUTLINE

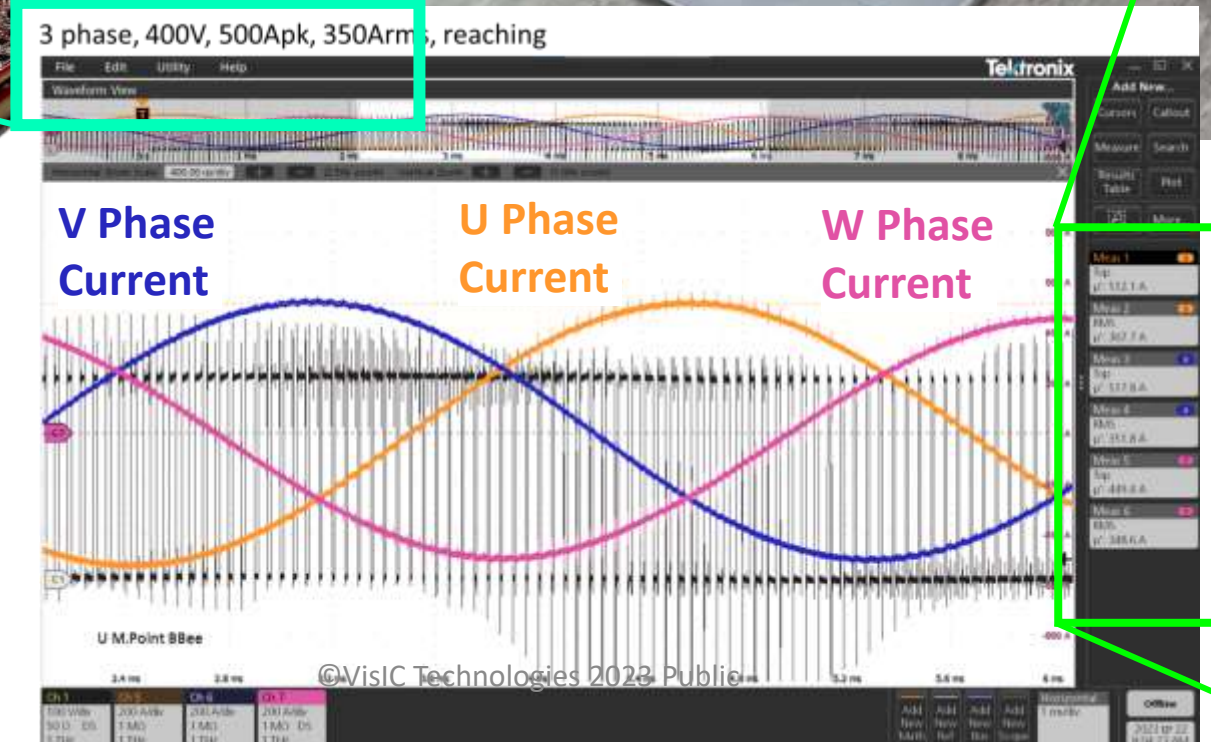
- Why GaN for 400V EV inverters?
- Challenges of inverter operation: transistor and system view
- Practical solutions and results
- 800V: is it possible for GaN?
- Summary and what comes next

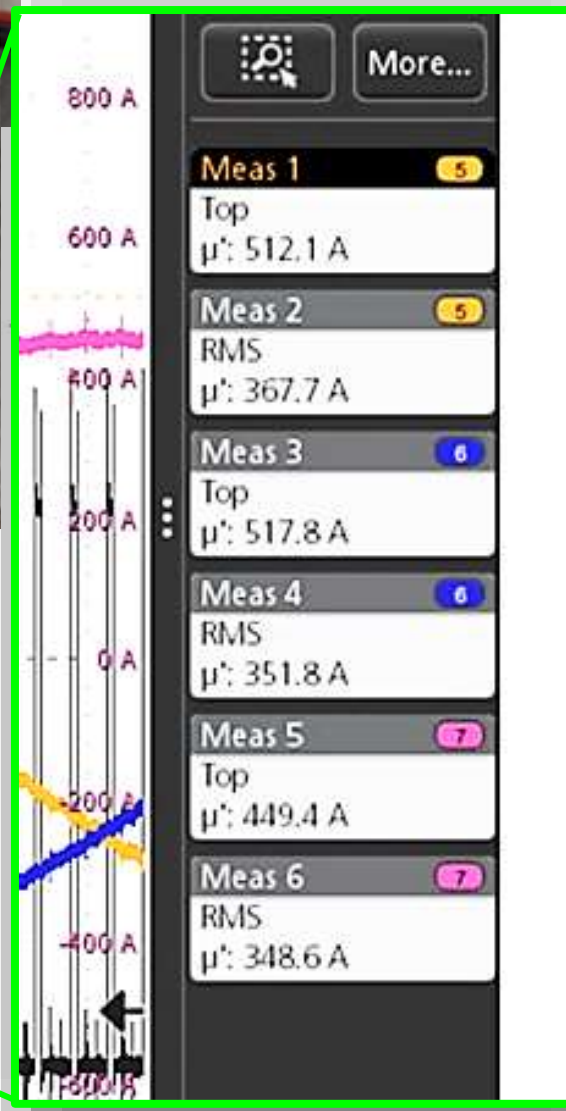
Is GaN for passenger car inverter possible?

Tested at OEM with motor









4 x 8 mOhm GaN die
2.2mΩ 650V HB D^{3}GaN

Power Module (& Driver

Module) Prototype,

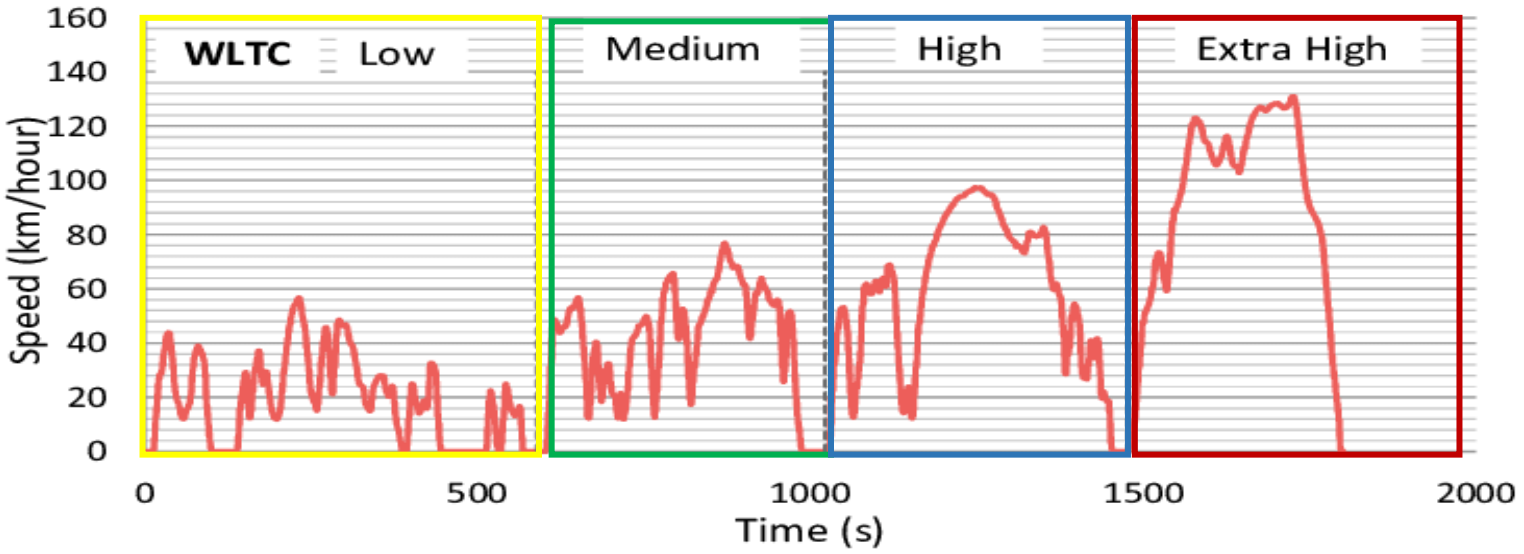
Based on VisIC V08 FETs

Fundamentals of Motor Inverter Operation

DRIVING CYCLE: set of conditions car experiencing during driving lifetime

WLTC Standard (Worldwide harmonized Light-duty vehicles Test Cycle) is the 30 min test for passenger cars and light commercial vehicles mimicking driving cycle to measure

- mean fuel consumption,
- CO_2 and other pollutants emissions
- EV car efficiency



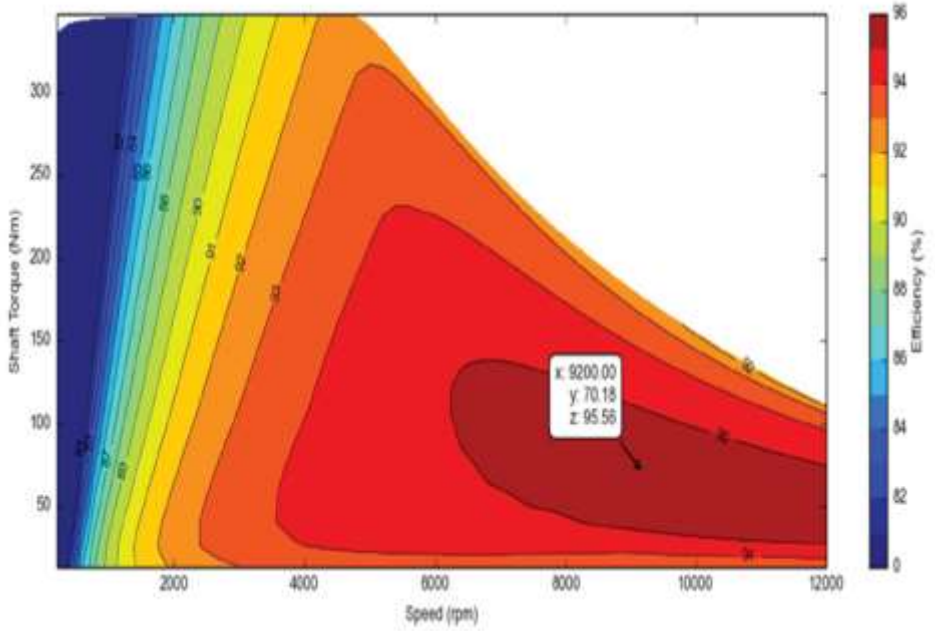
	WLTC
Duration (s)	1800
Total distance (km)	23.27
Average speed (km/h)	46.5
Maximum speed (km/h)	131.3
Stop duration (%)	13.00

Fundamentals of Inverter Operation: Efficiency

Inverters are made for peak load condition

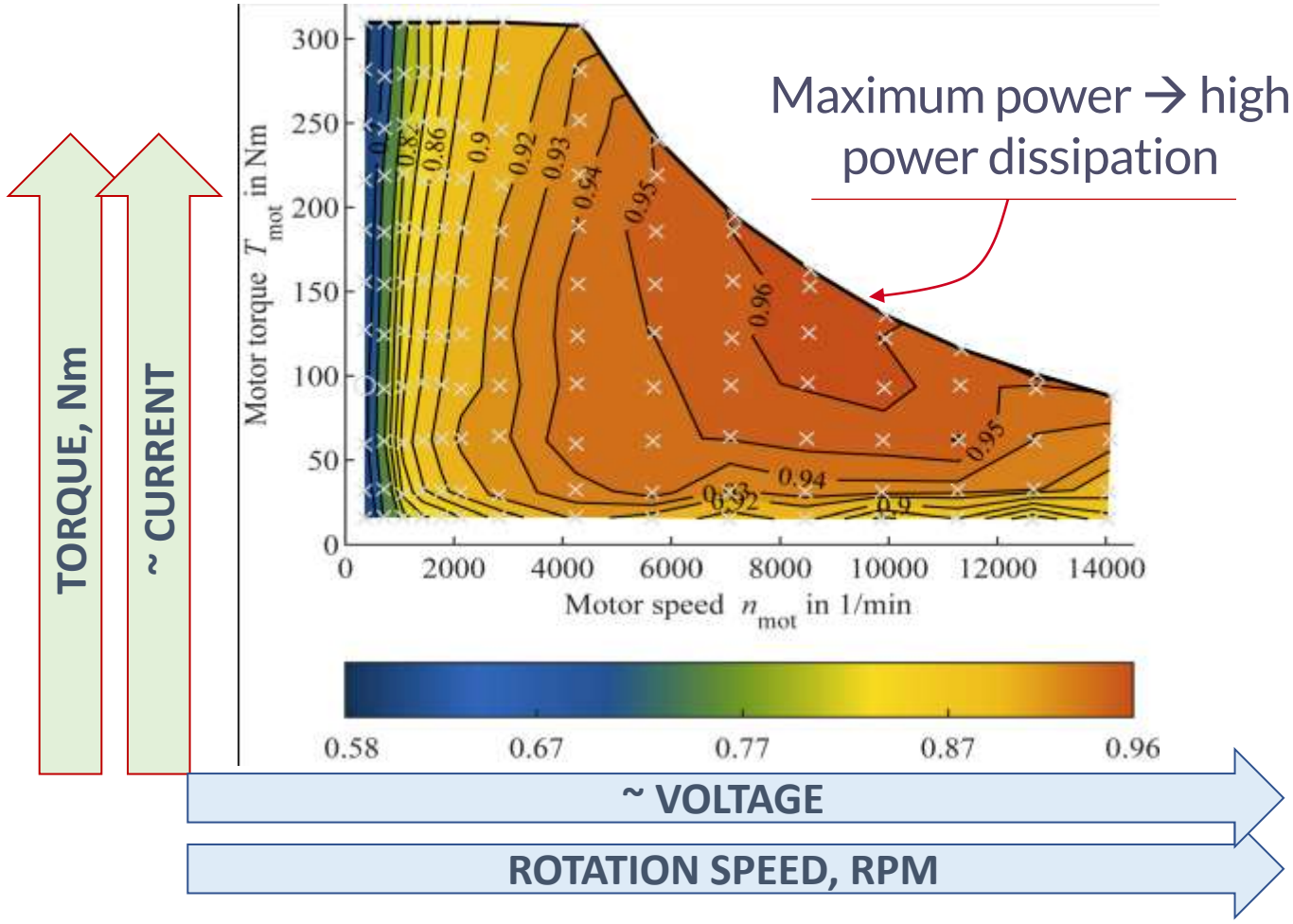
e.g. 150 kW – 250 kW

300 A – 500 A



Example of efficiency map of EM

https://www.motor-design.com/white-paper-ev-trade-off-analysis/



Efficiency map of Volkswagen ID.3,

Wassiliadis et al, eTransportation, Vol12, May '22, 100167

Fundamentals of Inverter Operation: Efficiency

SWITCHING LOSSES DICTATE INVERTER EFFICIENCY

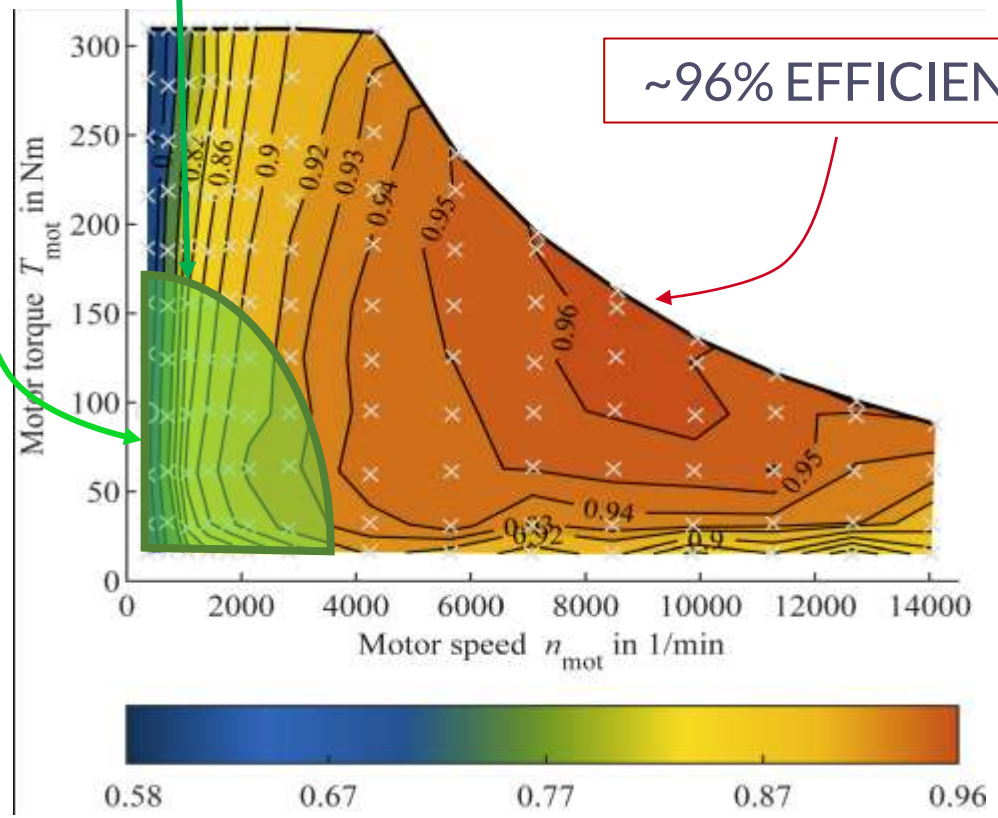
~75%-90% EFFICIENCY

Most of time we are driving here:

Low current →

Low conduction losses →

Dominant switching losses



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Fundamentals of Inverter Operation: Test data

ACTUAL TEST DATA

POWER LOSSES OVER WLTC

(DONE BY TIER-1)

20 kHz inverter

SYSTEM

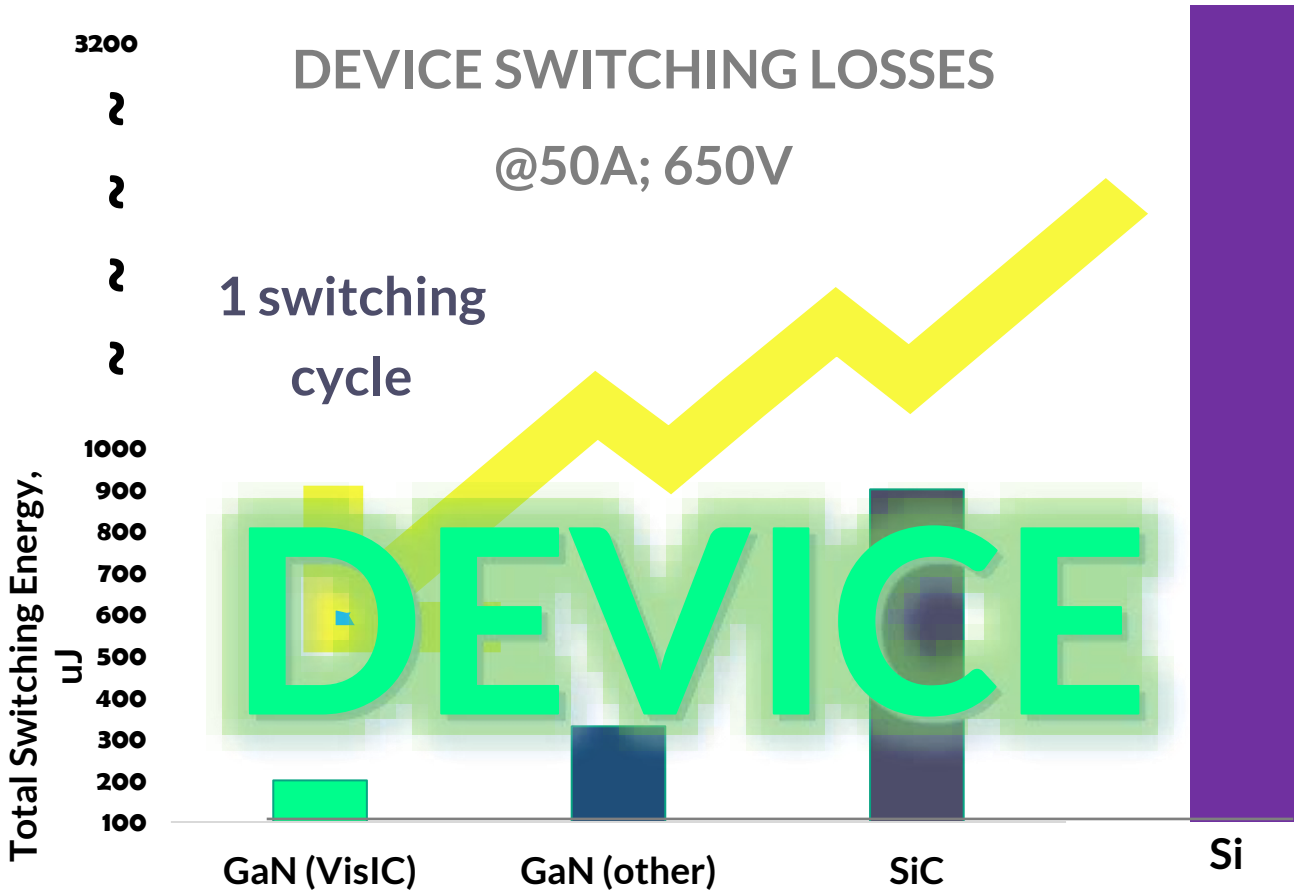
3 X lower losses than Si

2 X lower losses than SiC

DEVICE SWITCHING LOSSES

@50A; 650V

1 switching cycle

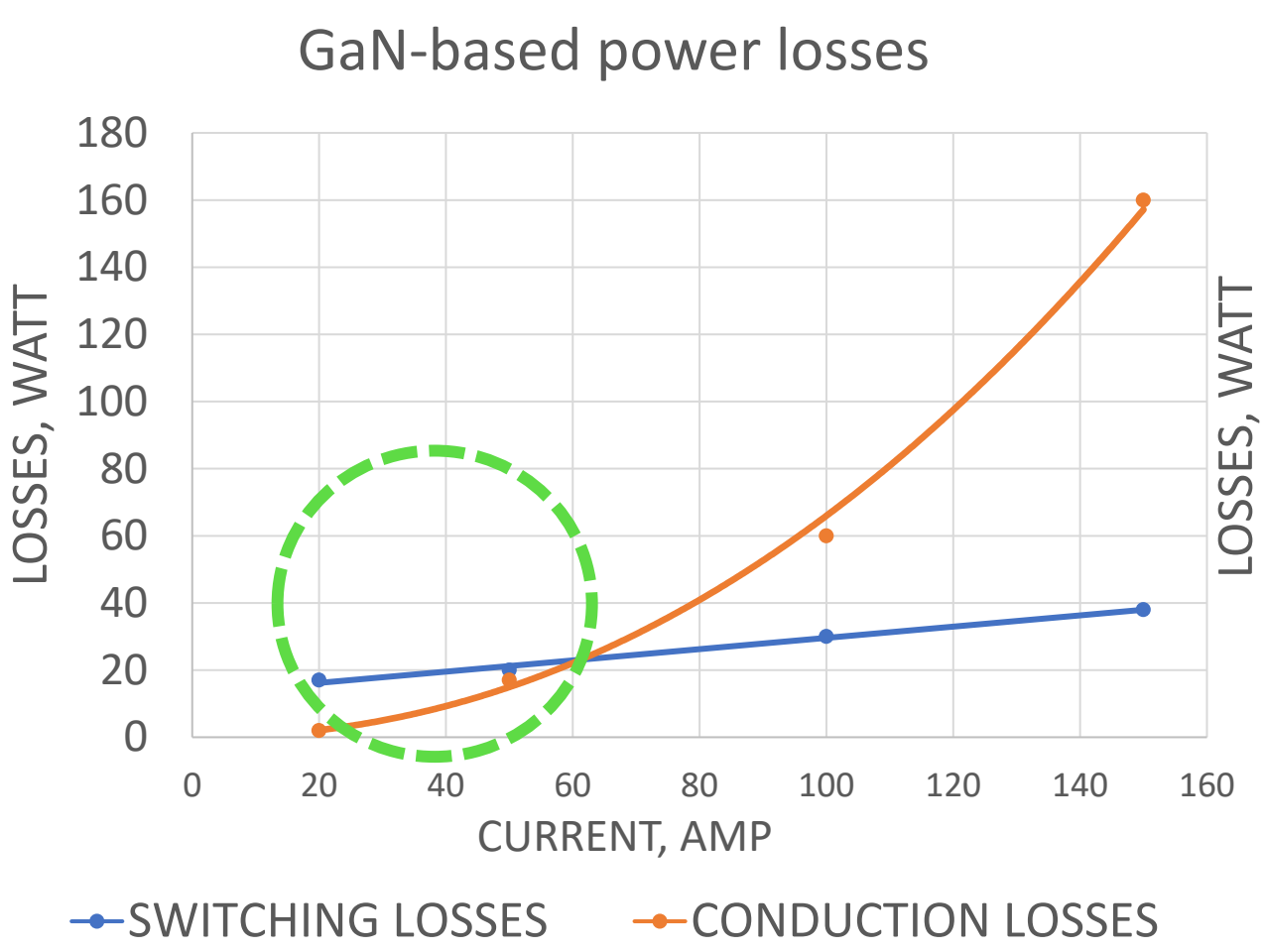


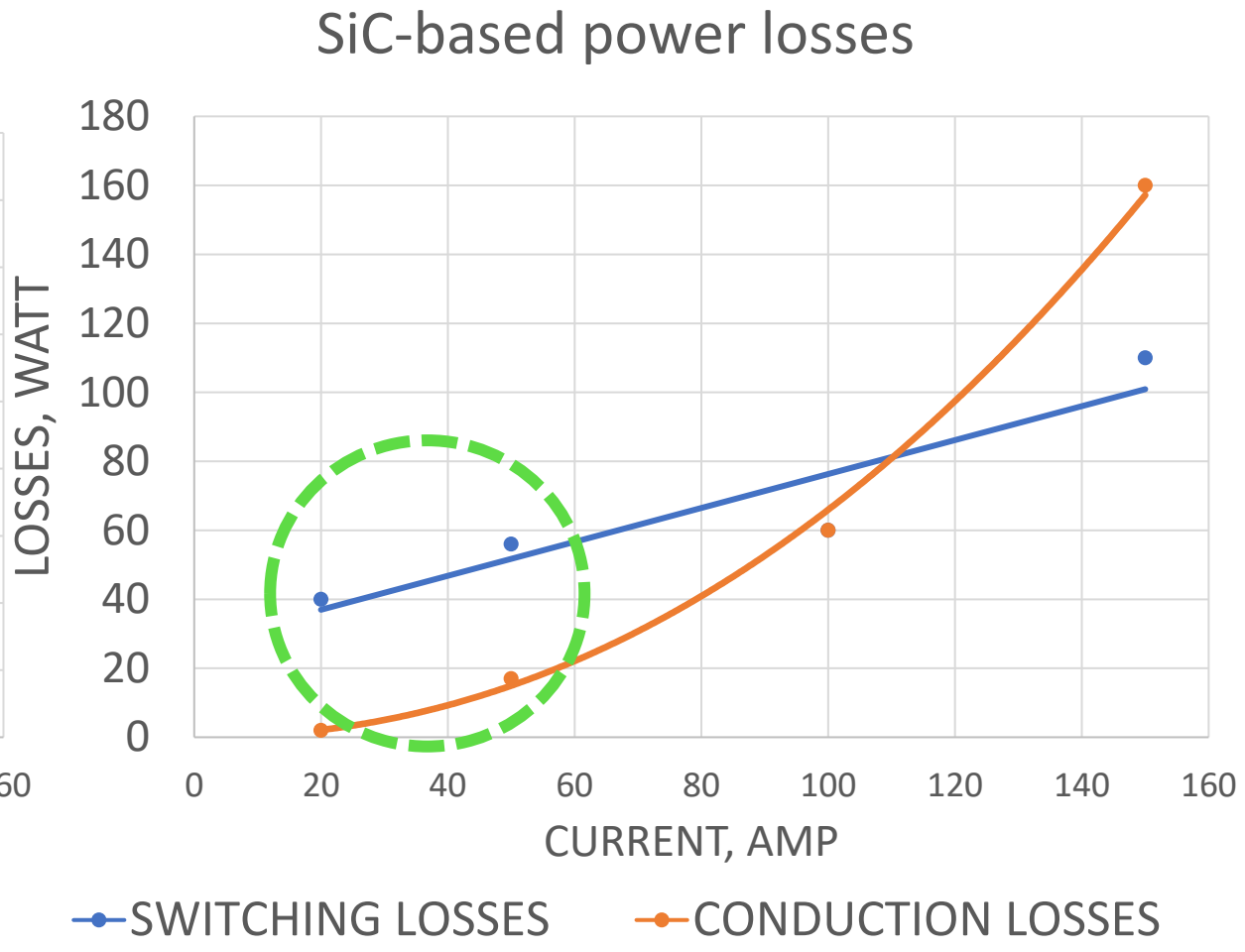
DEVICE

10 X lower losses than Si

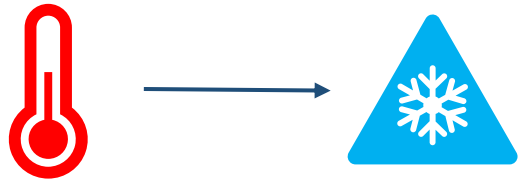
4.5 X lower losses than SiC

GaN Advantage depends on condition





Advantages of GaN based Highly Efficient Inverter



Car Cost Reduction
by battery shrink

Drive Distance Increase
by saving energy

Thermal Design Simplify
by shaving off heat

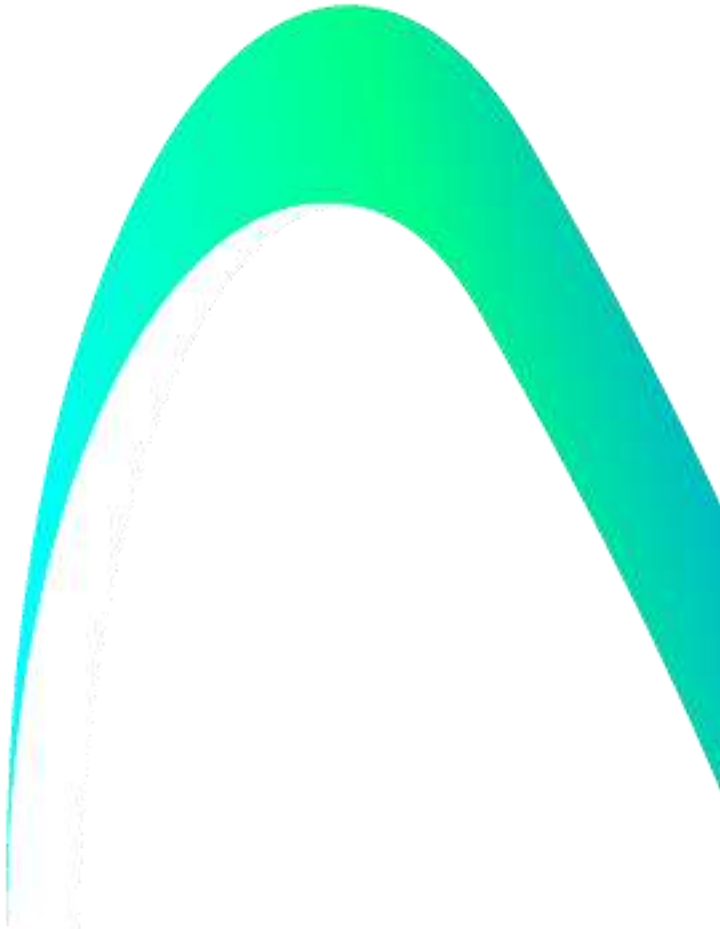
10%
Smaller battery

GaN
tailored for
inverters

10-20%
Longer range

Improving Inverter efficiency reduces battery size and increases driving distance

Challenges of EV inverter operation: from system to transistor



Device for EV power train

Target features:

- ❑ Reliable by automotive standards
- ❑ Process uniformity to produce high current dice (>100A) at high yield
- ❑ Low switching losses per given RDSON
- ❑ High threshold voltage (> 5V)
- ❑ Easily paralleled, 4-6 devices

Device design choice

DIRECT DRIVE

MISHEMT D-mode

D³GaN, VisIC

Integrated Driver, Texas Instruments

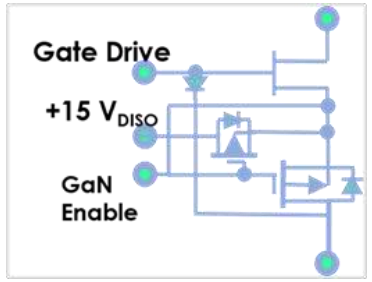
Cascode: IR (disc.) Transphorm, Nexperia

JFET or P-gate HEMT

E-mode TSMC, EPC, Panasonic, Infineon, Innoscience

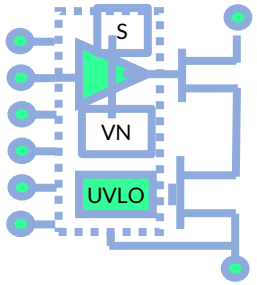
ADVANTAGES
- Low switching loss
- Robust Positive V_{TH}
- Low R_{ON}
- Easy paralleling
- Standard Si driver 0/+15

CONCERNS
- Package complexity



ADVANTAGES
-Low switching loss
-Driver integration with full protection

CONCERNS
-Low Power dissipation
-Complex paralleling
-Package complexity



ADVANTAGES
- Standard Si driver
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CONCERNS
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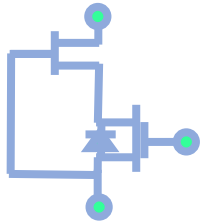
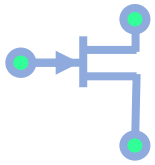
-Package complexity
-High LS inductance
-High switching losses



ADVANTAGES
- Easy paralleling
-Single die solution

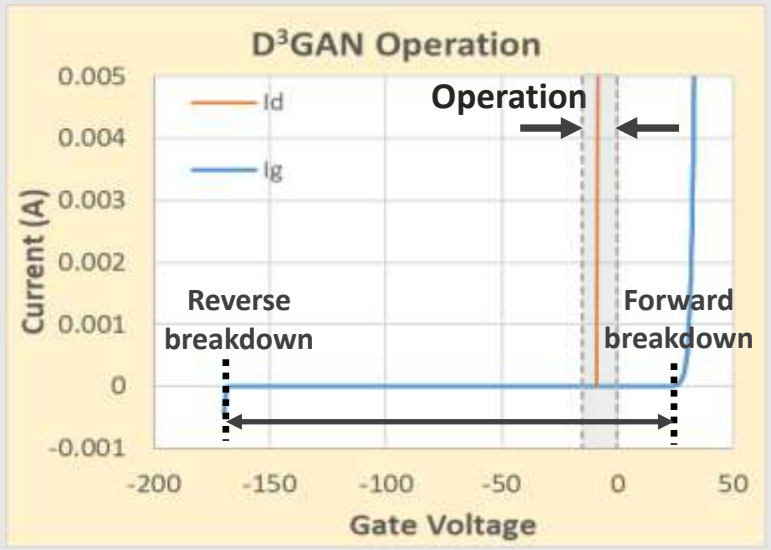
CONCERNS
-Low VTH
-Low gate isolation

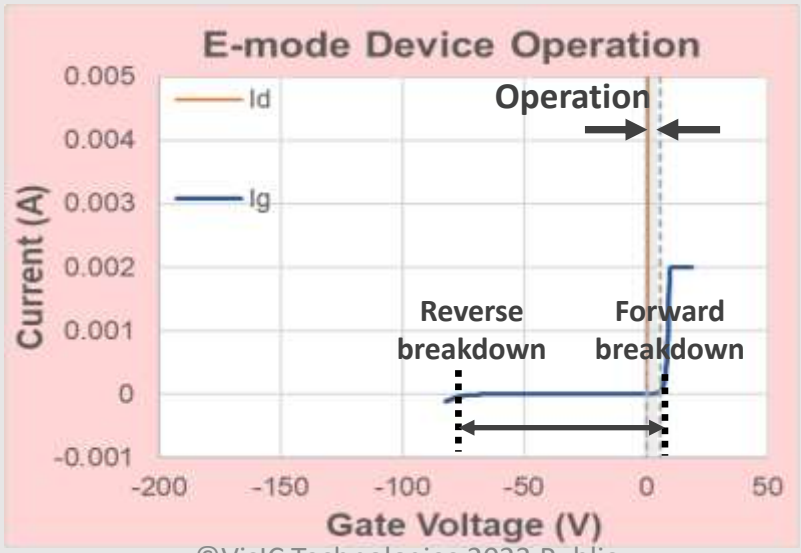


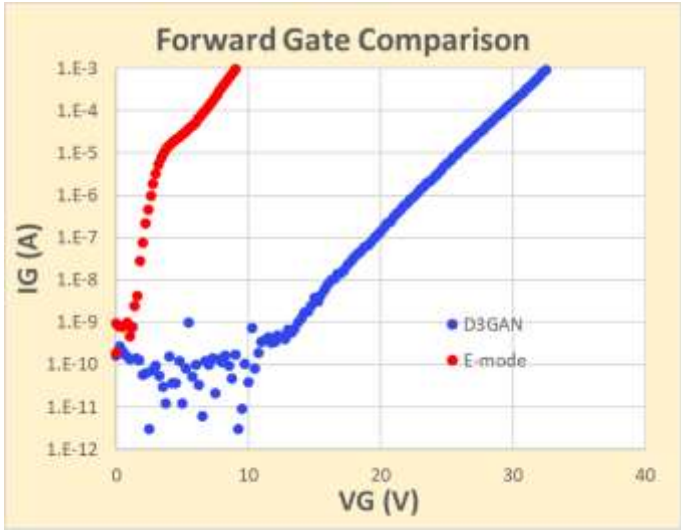
D-mode vs E-mode

1. D-mode is proven reliable technology widely employed in high power RADARs front end
2. D-mode has fundamentally lower specific R_{DSON} for same class, due to absence of V_T and R_{DRSON} trade off
3. D-mode has fundamentally better reliability and robustness due to absence of doping-introduced defects

Gate current versus Vgs[V] depicting operational region and gate breakdown







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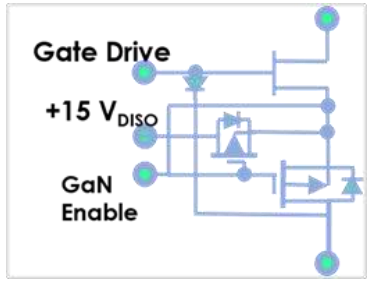

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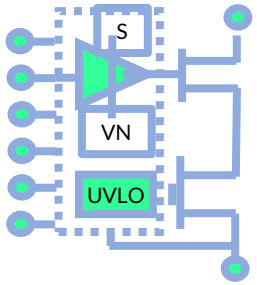

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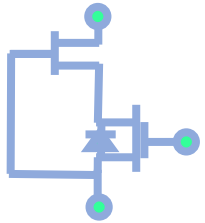

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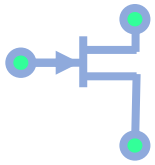
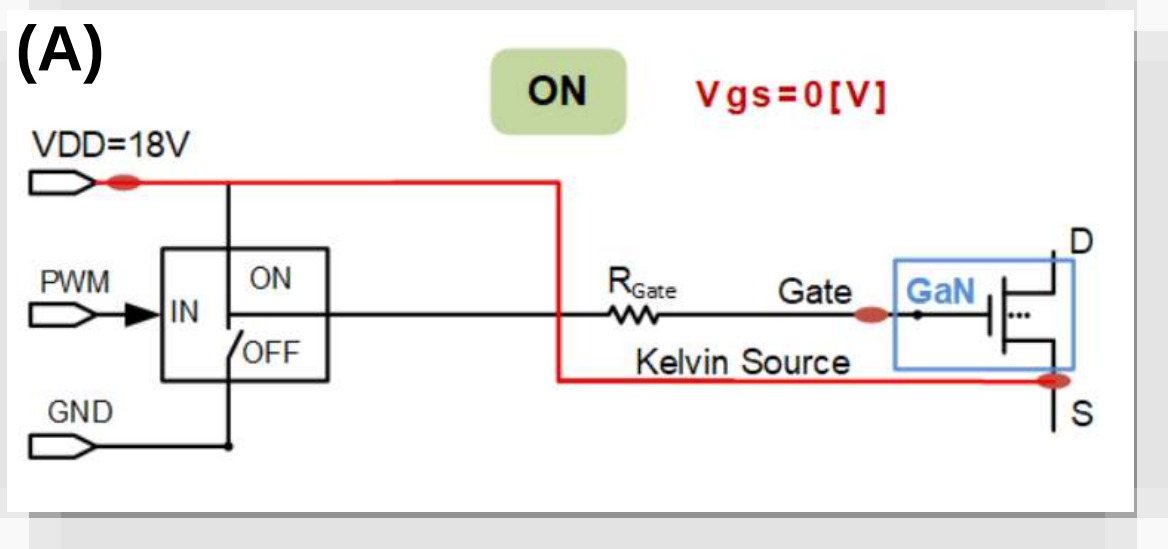
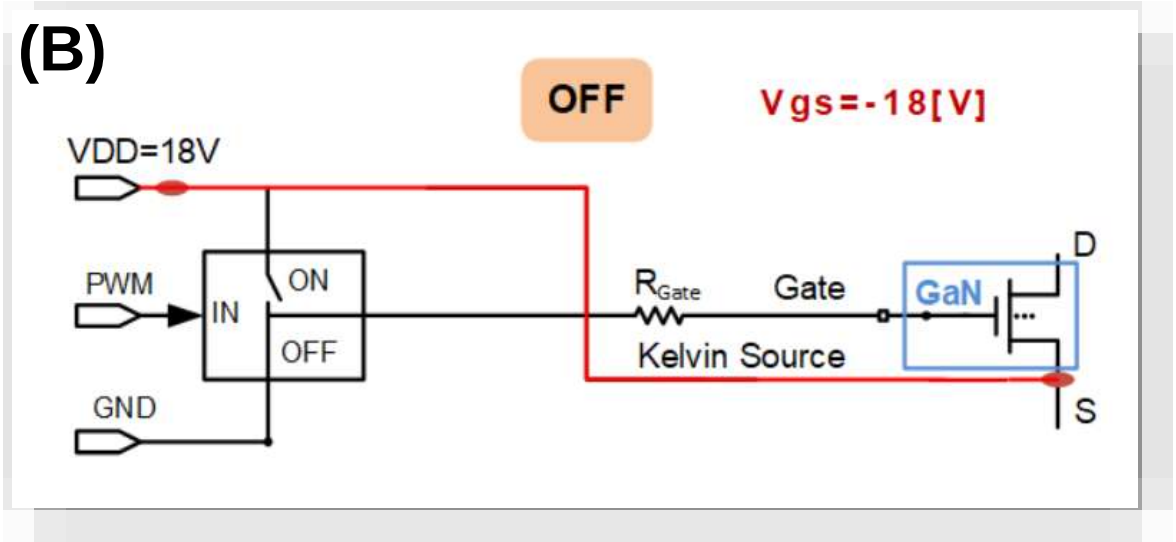


D3GaN – Direct Drive D-Mode GaN (1of2)

Gate – Source potential difference [Vgs] equals the difference of driver output potential and driver (VDD) potential.





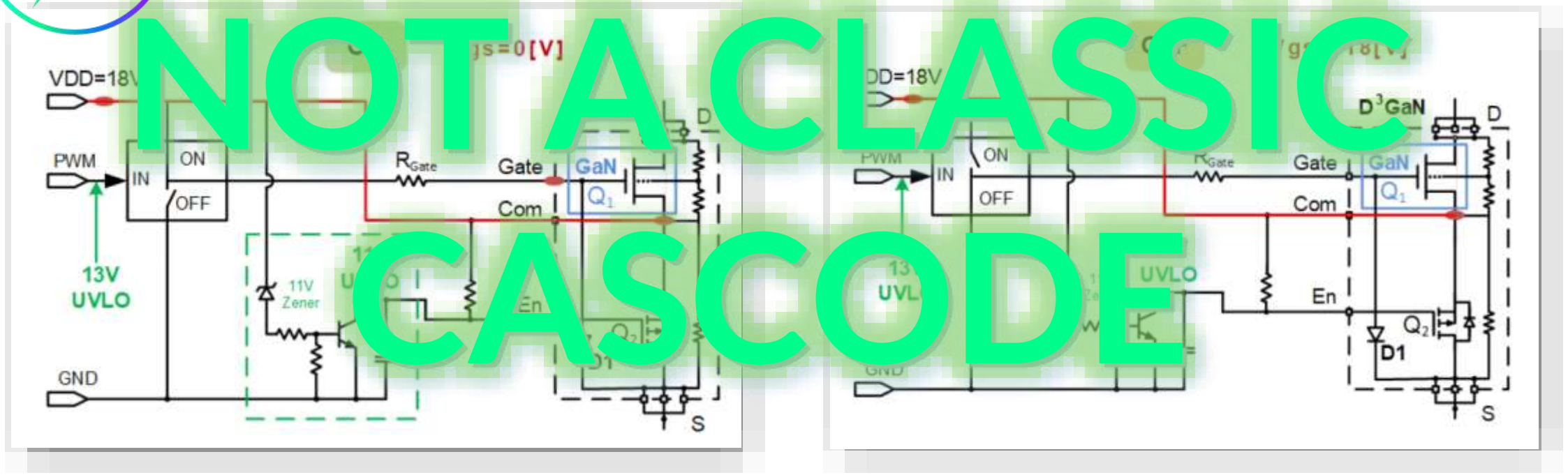
Threshold voltage of GaN is -8V, therefore when

- Gate to Kelvin potential is 0V, GaN device is conducting (**A**)
- Gate to Kelvin potential is -18V, GaN device is not conducting (**B**)

Effective Threshold Voltage is +10V

As SiC, D3GaN uses standard of-the-shelf gate drivers with a standard of-the-shelf Auxiliary Power Supply (VDD)

D3GaN – Direct Drive D-Mode GaN (2of2)

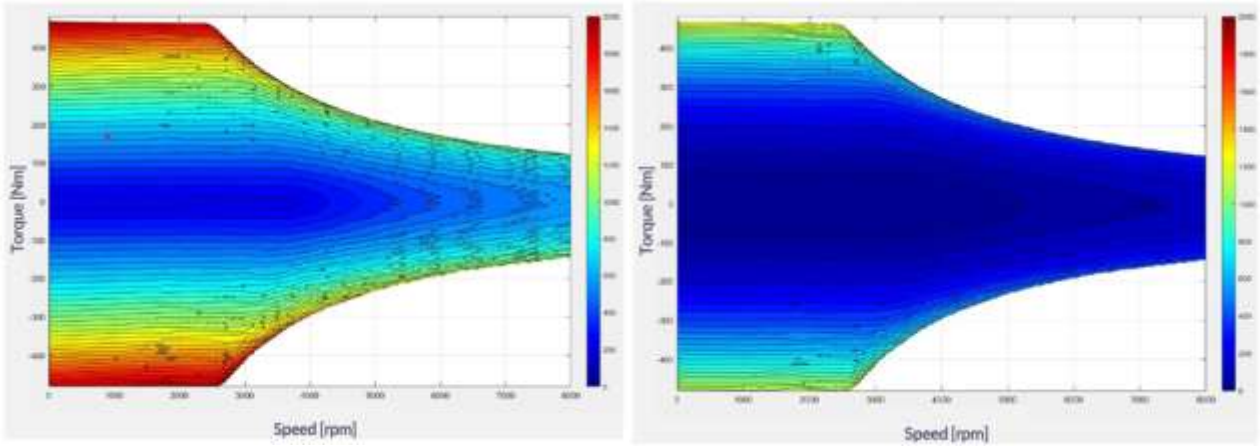


Q2 is ON when VDD is present and OFF when VDD is absent.
Q2 is not taking part in the switching process. It's held at "ON" during the switching of the D3GaN device

GaN for traction inverters

GaN is able for easy paralleling	→	High efficiency at high current
GaN's fast slew rate is controllable	→	Additional improvement with new e-motor
GaN for reliability	→	Robust technology & quality
GaN is scalable	→	800V designs are in progress

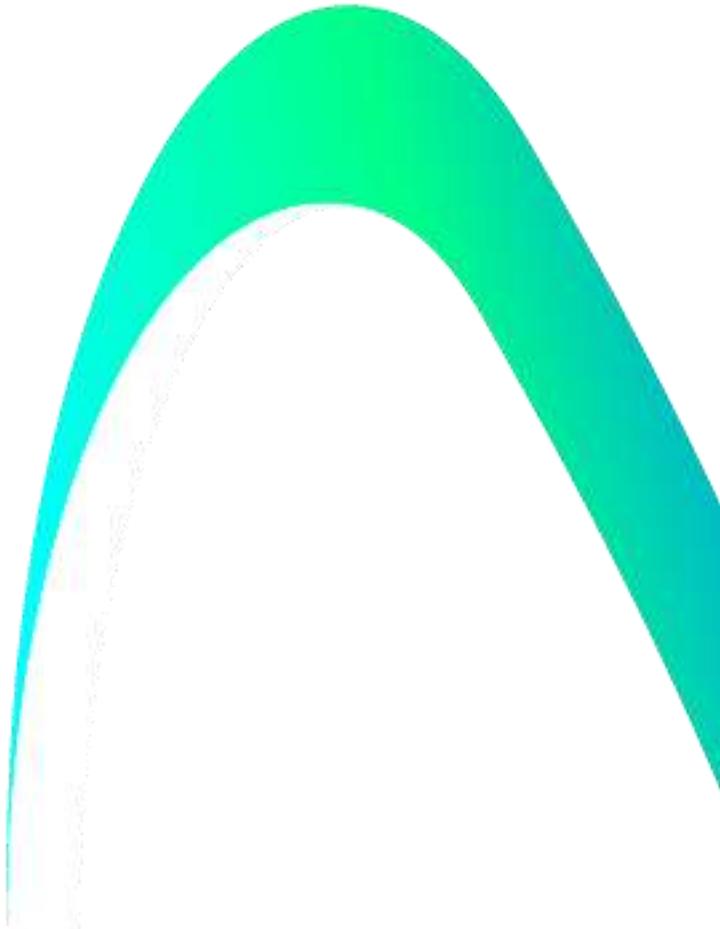
Inverter Power Loss Comparison
IGBT vs D³GaN



Source: major German automotive premium OEM

50% power loss reduction over the WLTP Driving Cycle

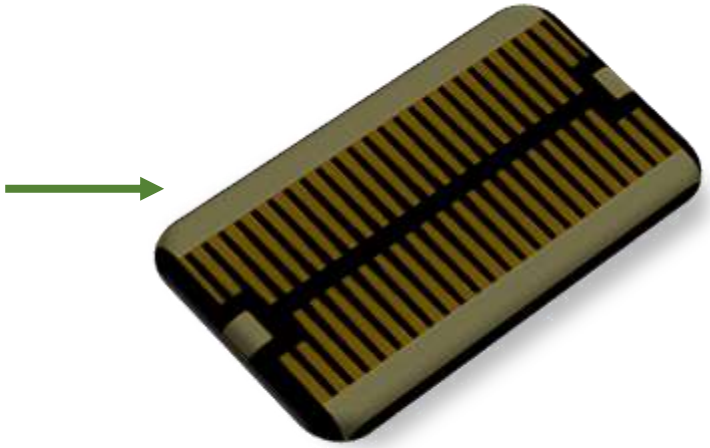
Practical solutions and results

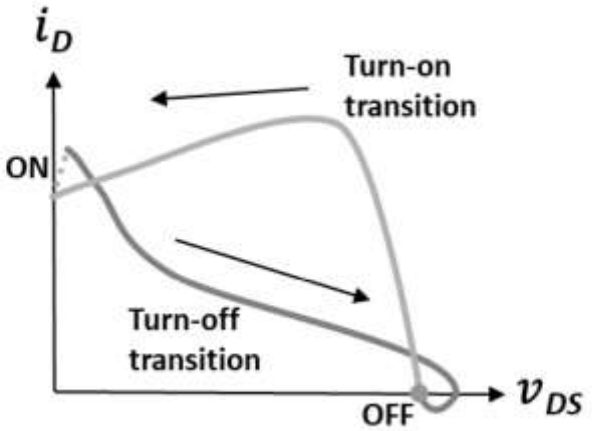


Main challenges

- INDUCTIVE LOAD SWITCHING: results in transistor switching loci with simultaneous high current and high voltage, which lead to high stress to device
- PARALLELING: High efficiency at high phase current requires multiple die paralleling, hence synchronous operation of multiple dice is required
- PARASITIC SIGNALS & SPIKES CONTROL : must be managed without increasing power losses
- SLEW RATE CONTROL: Customers need to control slew rate from 10 to 30 V/ns, with option up to 50 V/ns. High transconductance of GaN HEMT makes it challenging

Main challenges: Inductive load switching

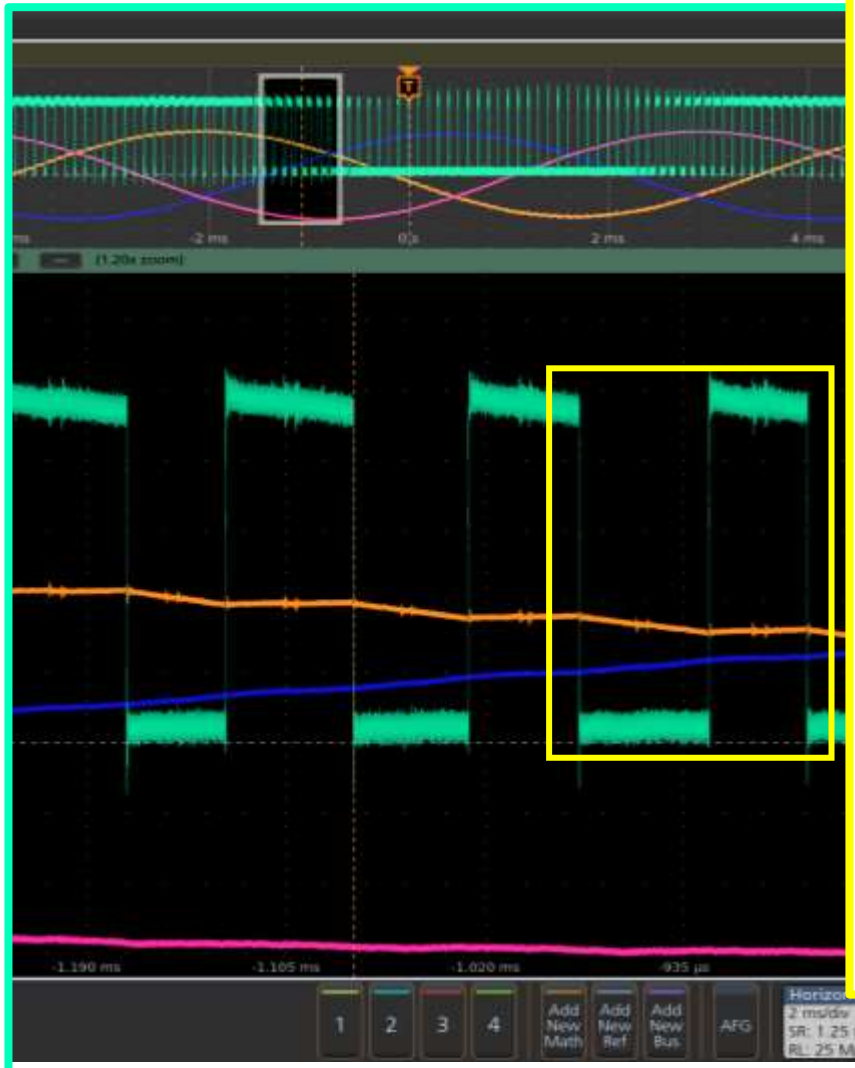


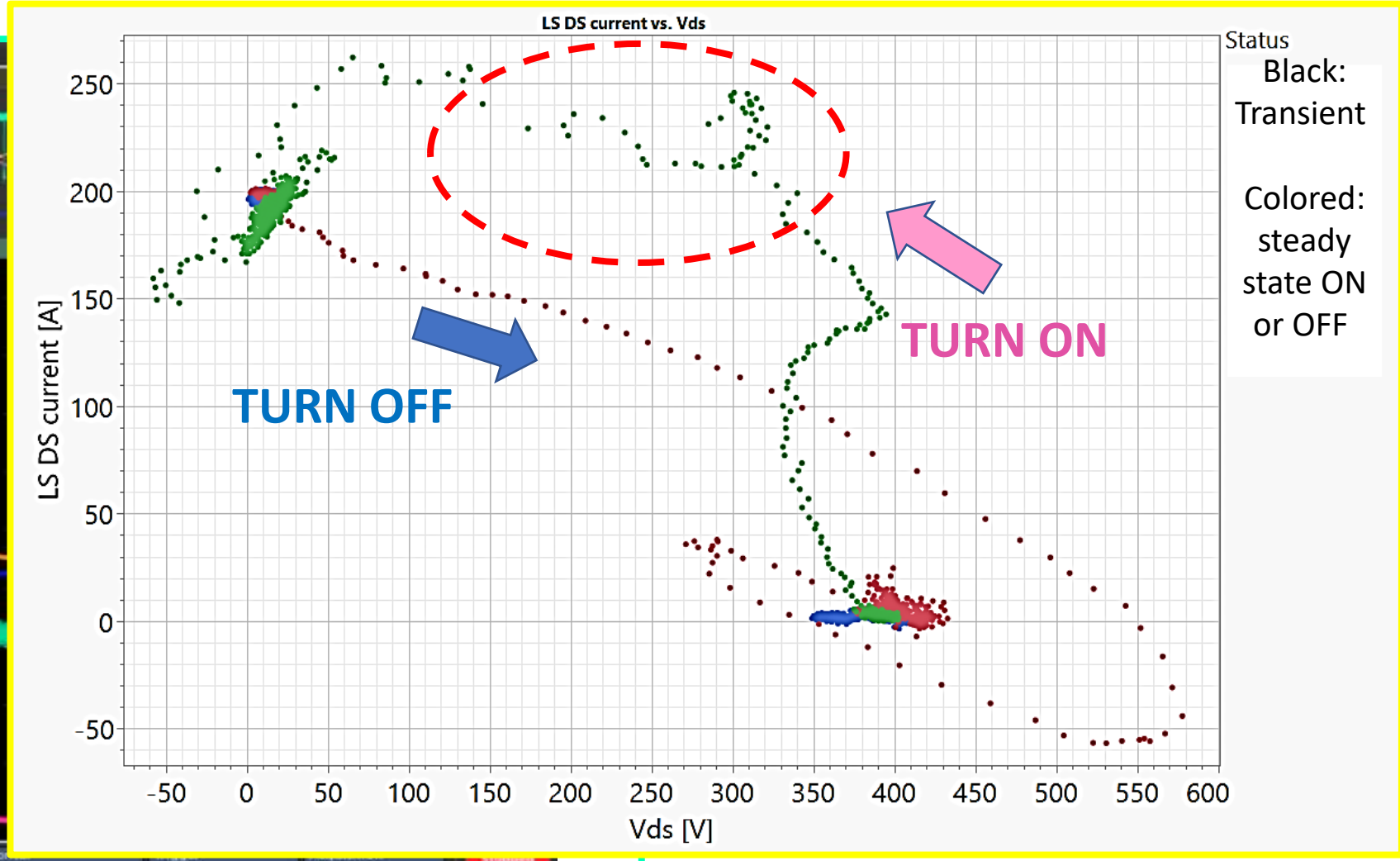


JEP 182, ver 1.0, page 9

- JEDEC standard JEP 182 provides guidelines for switching tests for GaN, with emphasis on right switching conditions
- Specific testing procedures which stress transistor in relevant conditions are required to optimize these transistors

Main challenges: Inductive load switching

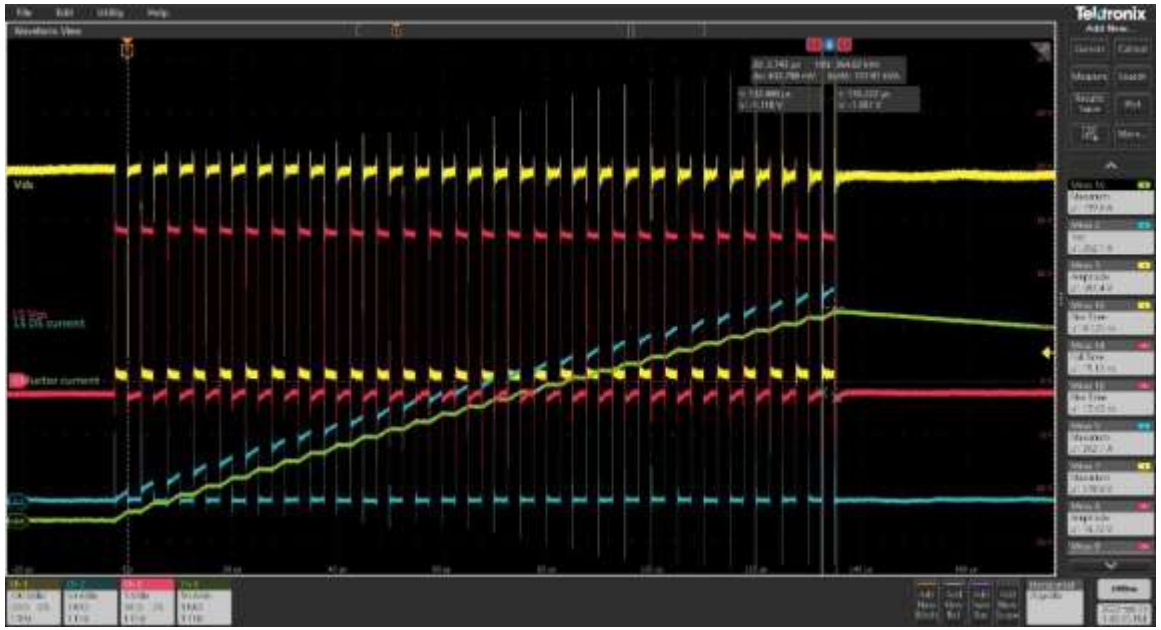


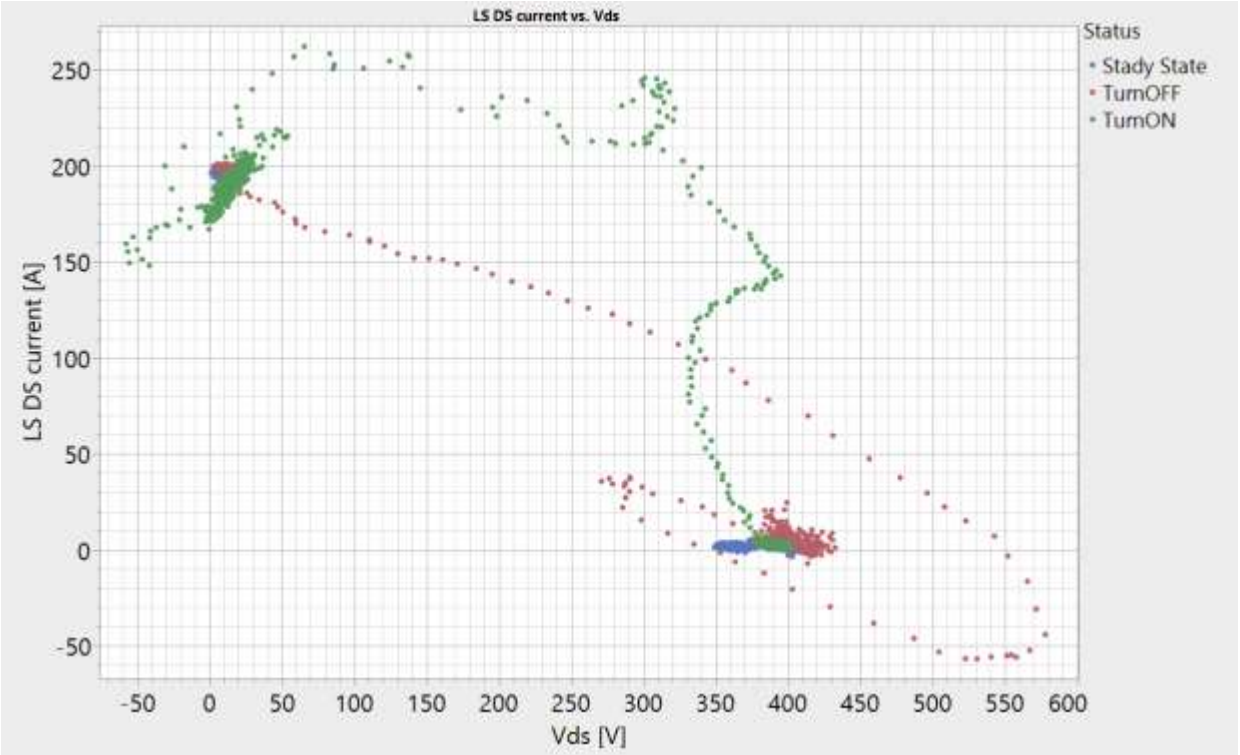


Inductive load switching: screening

Multi-pulse continuous test of HB with relevant current value, externally heated to 125°C

Duration 60 minutes



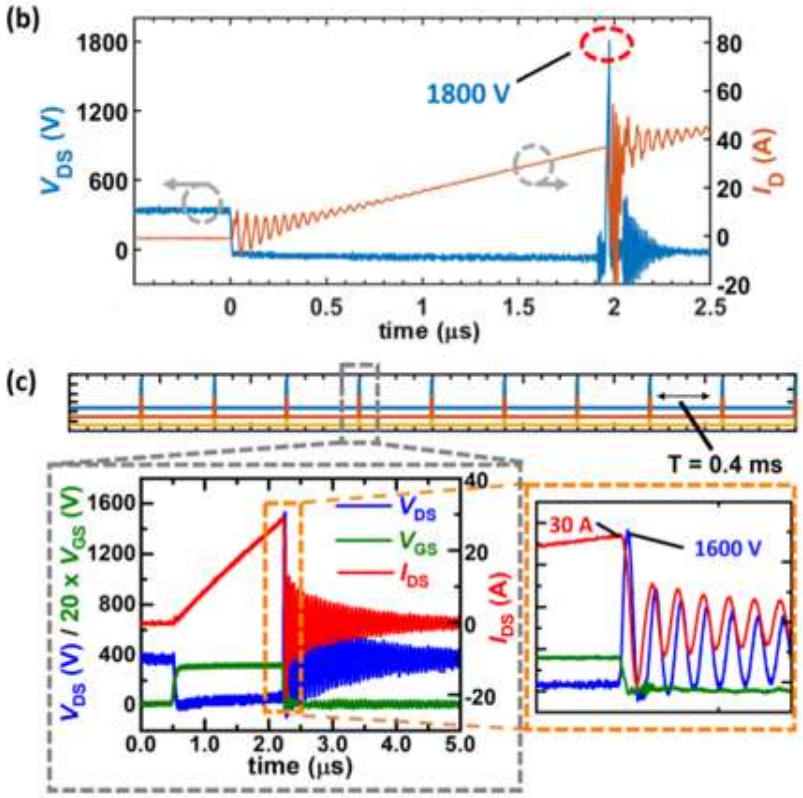


Screening of weak devices

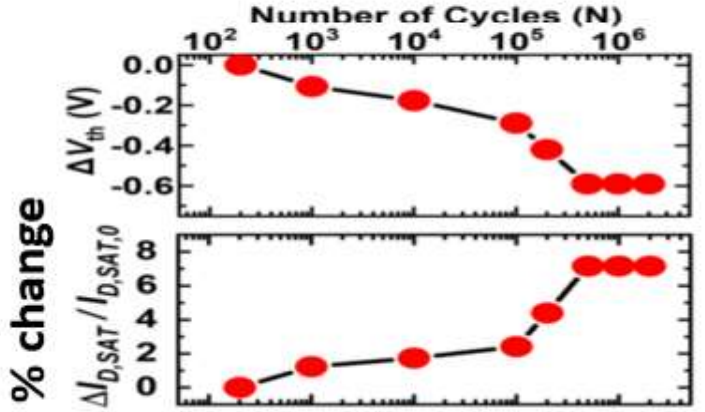
Inductive load switching: alternative approach

Alternative tests developed in CPES, Virginia Tech, to characterize readiness of GaN for EV inverter

LC resonant circuit using transistors's Coss helps to measure dynamic breakdown of the transistor and evaluate it's robustness in similar to inverter operation stress condition



- Repetitive pulses at **90% of dyn BV voltage (unparalleled capability: competitor technology were at ~50% for d-mode and ~25% for e-mode).**
- Negligible parametric shift were observed.
- Parametric results saturated after 1 million cycles.



Q. Song et al., "GaN MIS-HEMTs in Repetitive Overvoltage Switching: Parametric Shift and Recovery," 2022 IEEE International Reliability Physics Symposium (IRPS), Dallas, TX, USA, 2022, pp. 10B.4-1-10B.4-7, doi: 10.1109/IRPS48227.2022.9764548.

Paralleling of multiple devices

Main objective is a timing synchronization which is required to ensure proper current sharing between devices

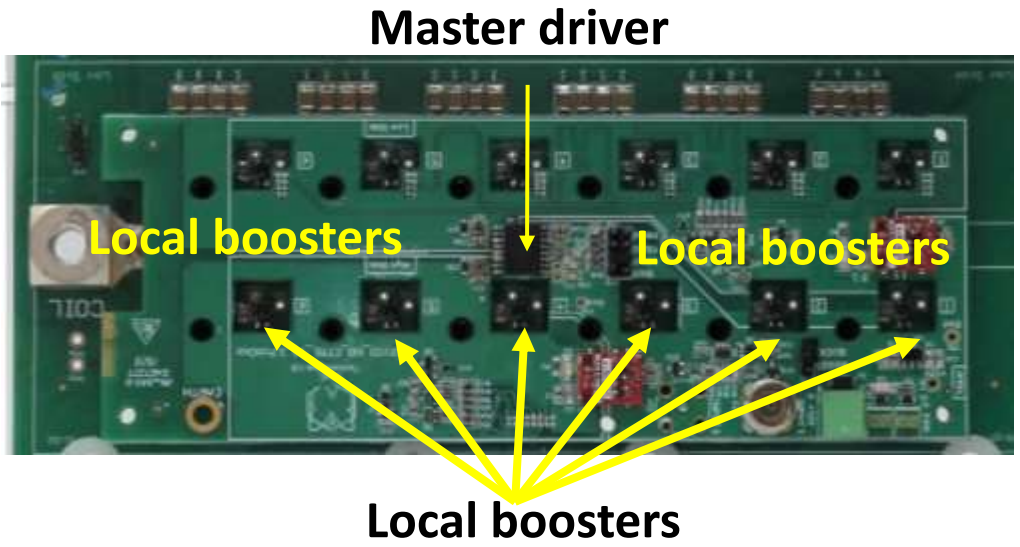
System of parallel devices:

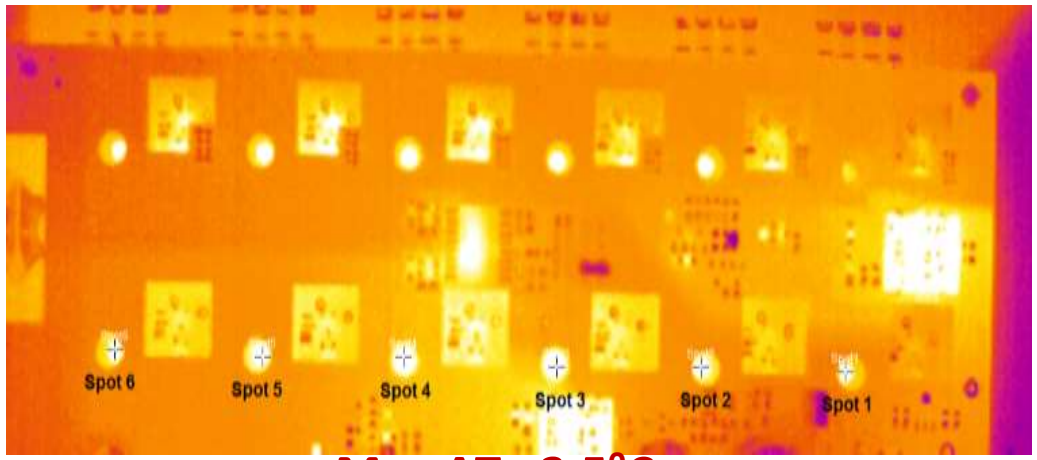
- Demands higher driver current
- More parasitic loops in the system
- Has higher gain value

More prone to oscillations, requires careful layout

Paralleling of multiple devices: driver consideration

Use one Master and few boosters

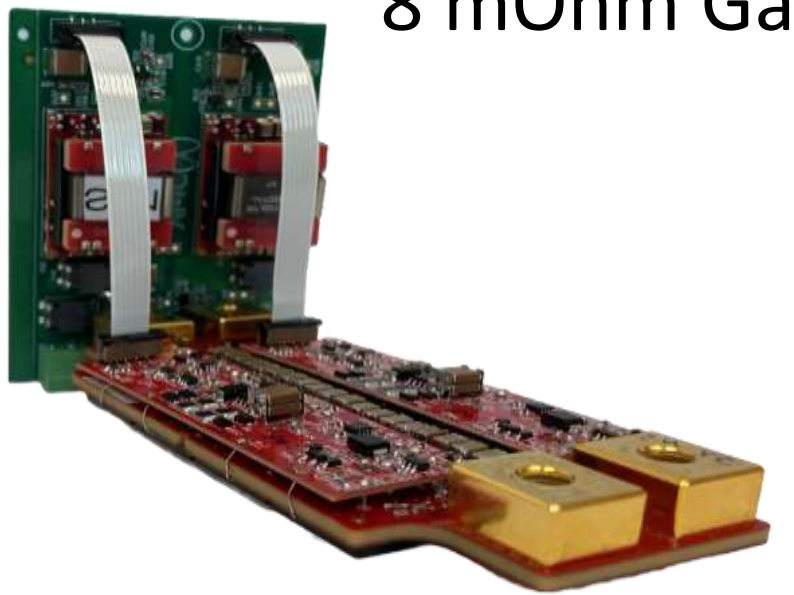




Max ΔT =3.5^{0}C

Use a two matched power driver chips in one package driver, e.g. 2ED24427 that has two 10 Amp matched drivers

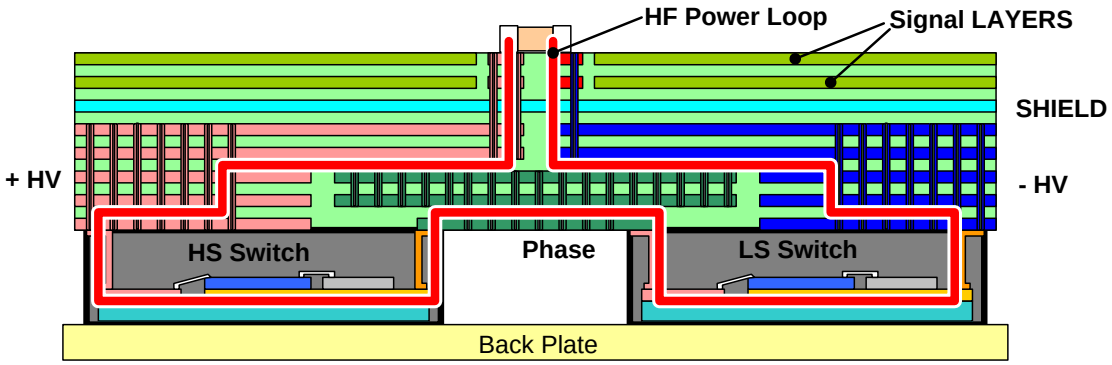
Each driver drives two 8 mOhm GaN devices



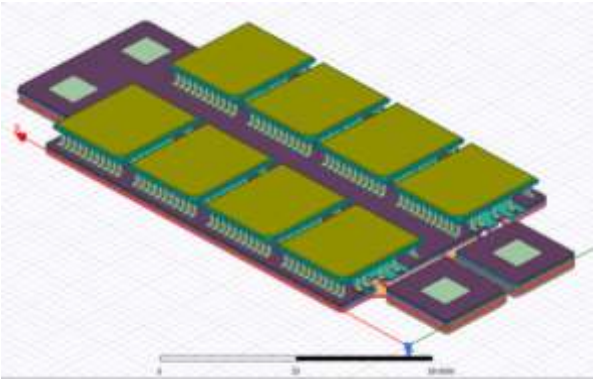
Paralleling of multiple devices: layout design

MAIN STEPS

1. Inductance reduction by minimizing the area enclosed by Power Loop
2. Increase current capability by adding layers and increasing Cu thickness
3. Decrease of capacitive coupling between phase terminal and rest of the circuit:
   by configuration of phase terminal
4. Reduction of HF noise coupling to control/driver circuits:
   by partitioning of functional areas, shielding

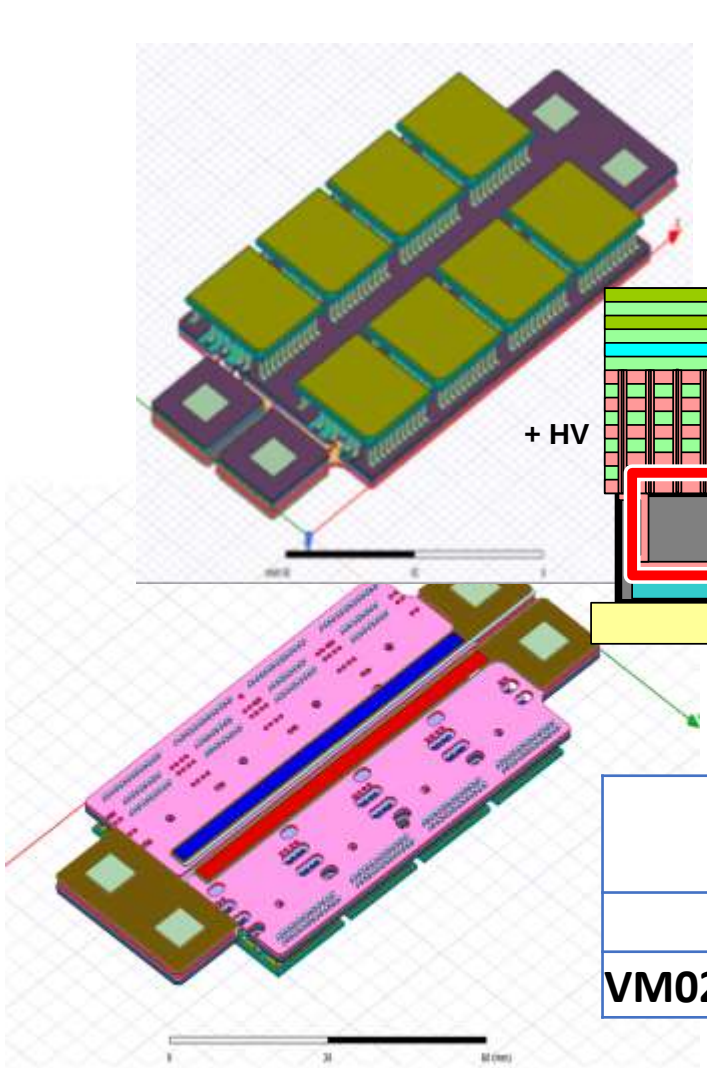


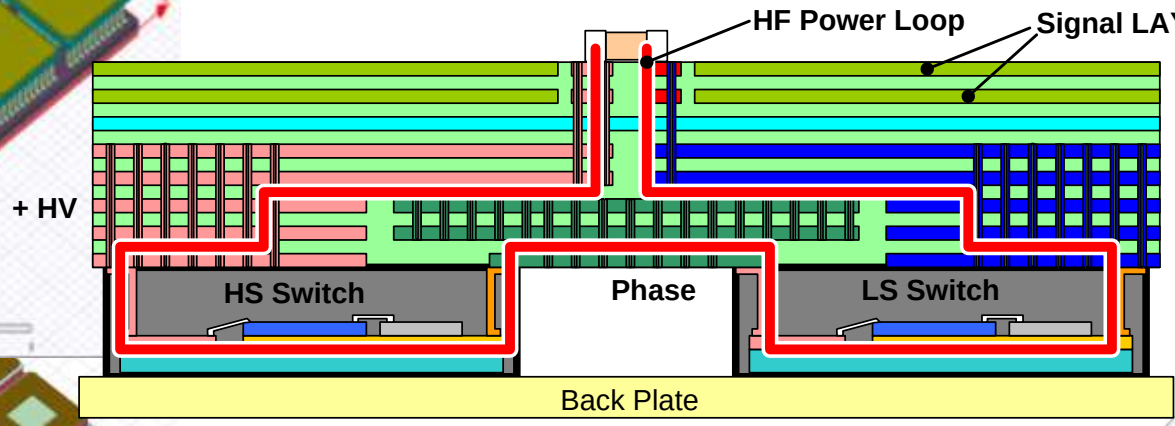
	Trace capacitance C[pF]		Stray Inductance L[nH]
	+HV'-Phase	-HV' -Phase	
VM022	235	240	1.87

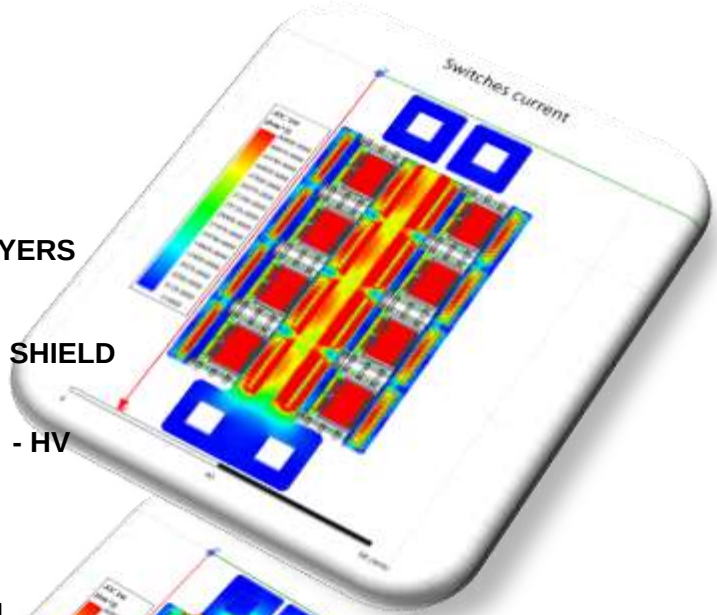


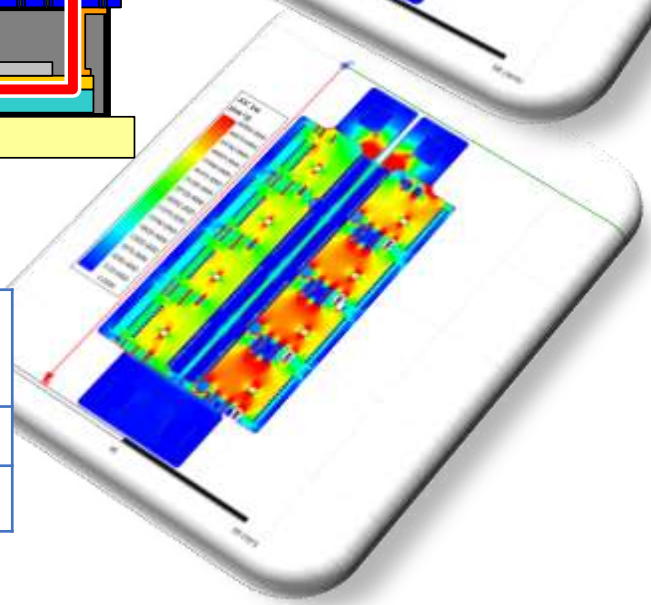
Paralleling of multiple devices: layout design

Layout→ EM simulation→ Optimization → Repeat → Manufacture --> Test --> Calibrate --> Repeat All









	Trace capacitance C[pF]		Stray Inductance L[nH]
	+HV'-Phase	-HV' -Phase	
VM022	235	240	1.87

Paralleling of multiple devices: layout design

Layout→ EM simulation→ Optimization → Repeat → Manufacture --> Test --> Calibrate --> Repeat All

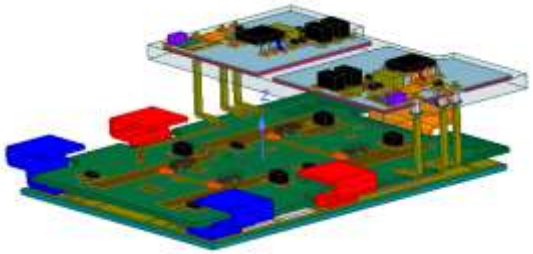
Power Loop

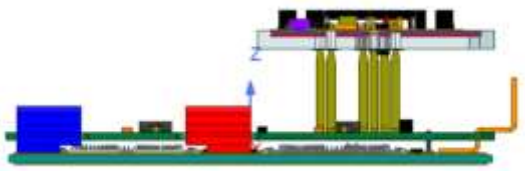
Clamping Loop

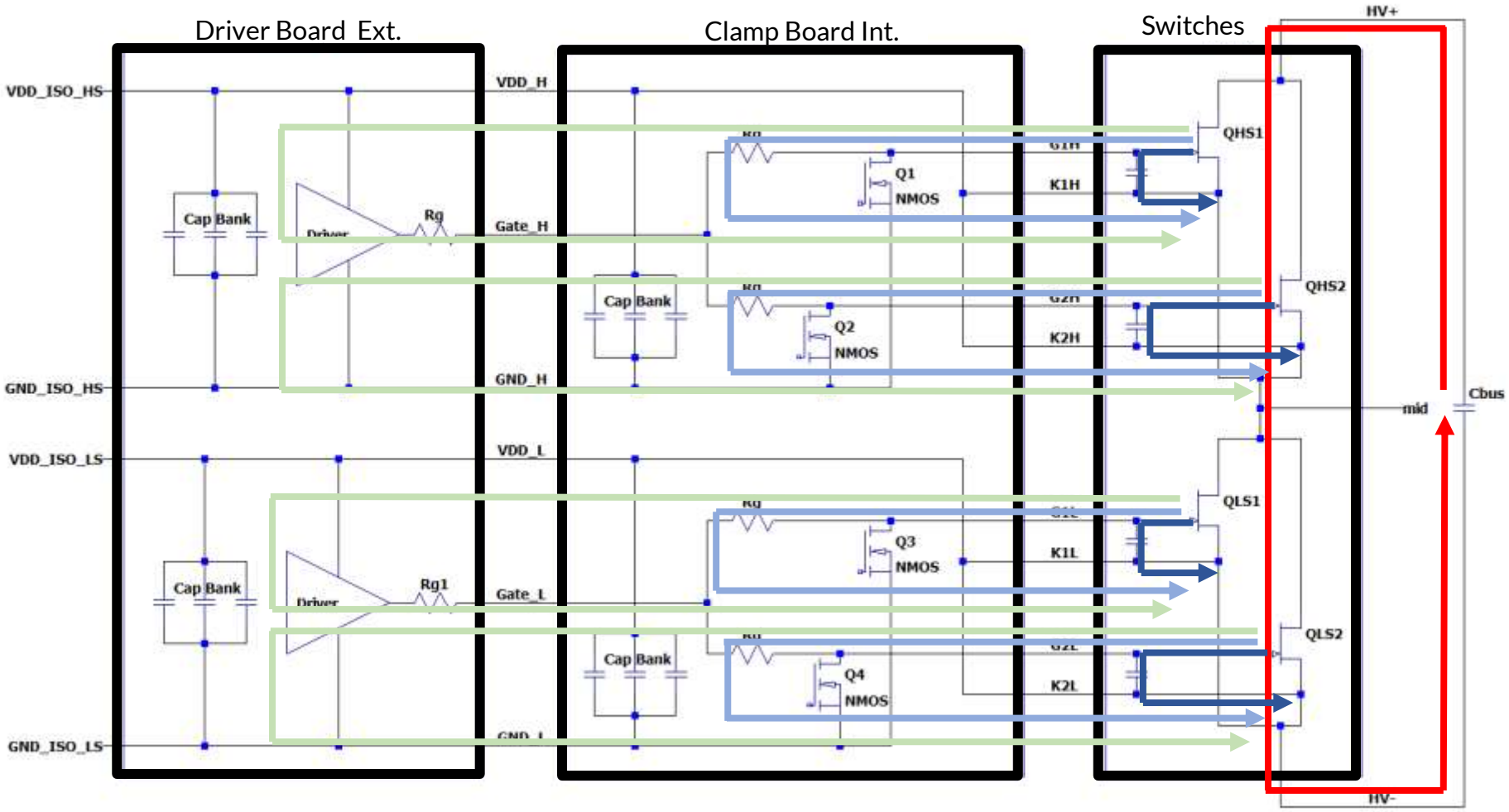
Driver Loop

Turn ON
Turn OFF

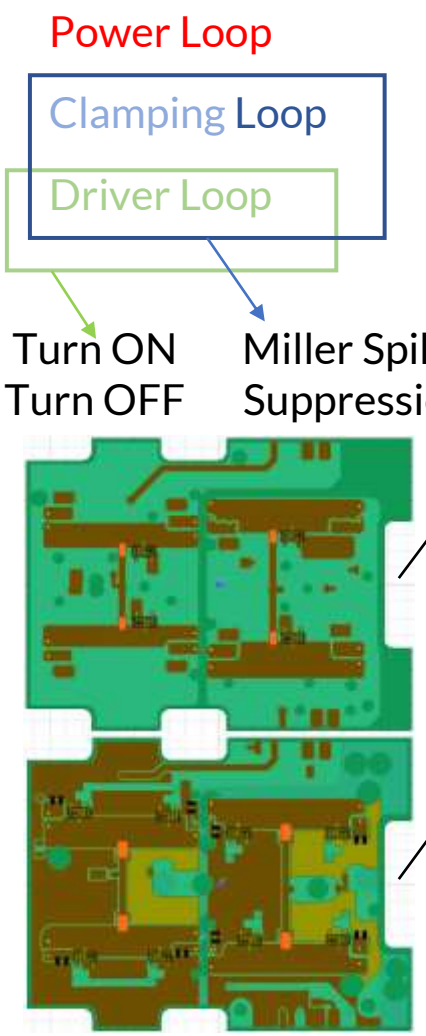
Miller Spike
Suppression







Paralleling of multiple devices: layout design



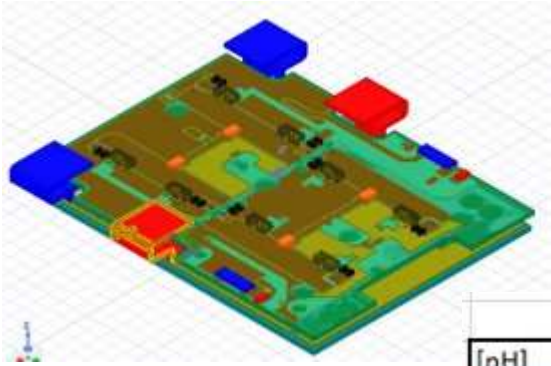
Inductance

		DRV+Clamp+C int.			DRV+Clamp			Driver Only		
Single Clamp	[nH]	Power	GH	GL	Power	GH	GL	Power	GH	GL
	Power	5.86346	0.0567	0.0384	5.84369	0.05452	0.04686	6.15471	0.06578	0.05773
	GH	0.0567	0.44855	0.01961	0.05452	1.52836	0.01618	0.06578	16.639	0.03663
	GL	0.0384	0.01961	0.45069	0.04686	0.01618	1.57882	0.05773	0.03663	18.8811

		DRV+Clamp+C int.			DRV+Clamp			Driver Only		
Dual Clamp	[nH]	Power	GH	GL	Power	GH	GL	Power	GH	GL
	Power	5.78521	0.05645	0.03641	5.79212	0.0552	0.02044	6.15471	0.06578	0.05773
	GH	0.05645	0.44398	0.0194	0.0552	1.16216	0.01451	0.06578	16.639	0.03663
	GL	0.03641	0.0194	0.44685	0.02044	0.01451	1.15538	0.05773	0.03663	18.8811

Capacitance

[pF]	Power	GH	GL
Power	414.919	90.8815	124.939
GH	90.8815	109.74	4.51449
GL	124.939	4.51449	144.749



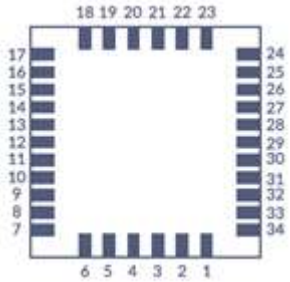
	Ideal Driver Board		
[nH]	Power	GH	GL
Power	5.8149	0.06891	0.04455
GH	0.06891	6.87061	0.00852
GL	0.04455	0.00852	3.98402

* Inductive coupling needs more work

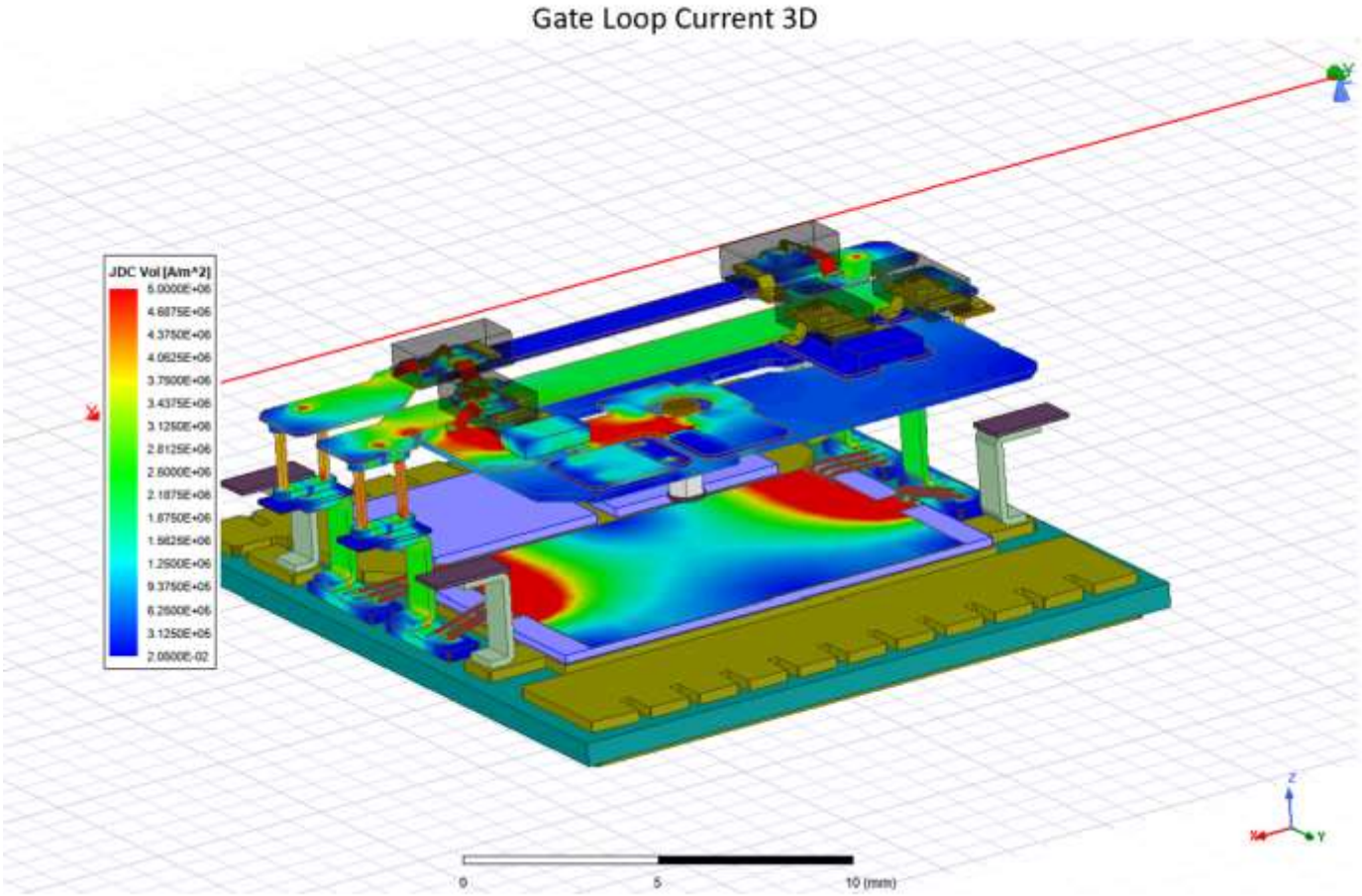
Gate loop: layout design

Layout→ EM simulation→ Optimization → Repeat → Manufacture --> Test --> Calibrate --> Repeat All

7mOhm/200A/650V

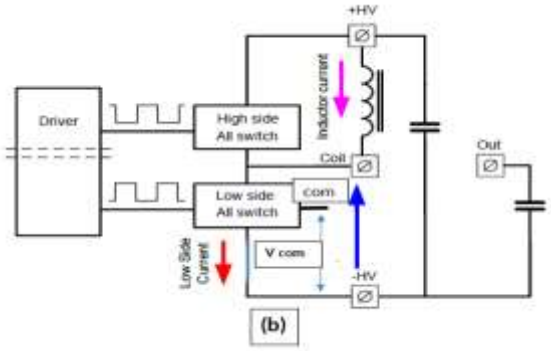


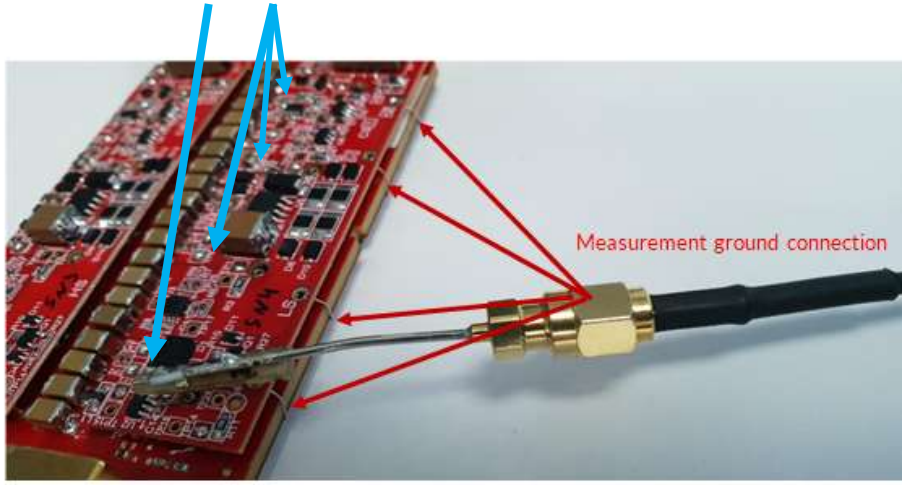
8mOhm/200A/650V



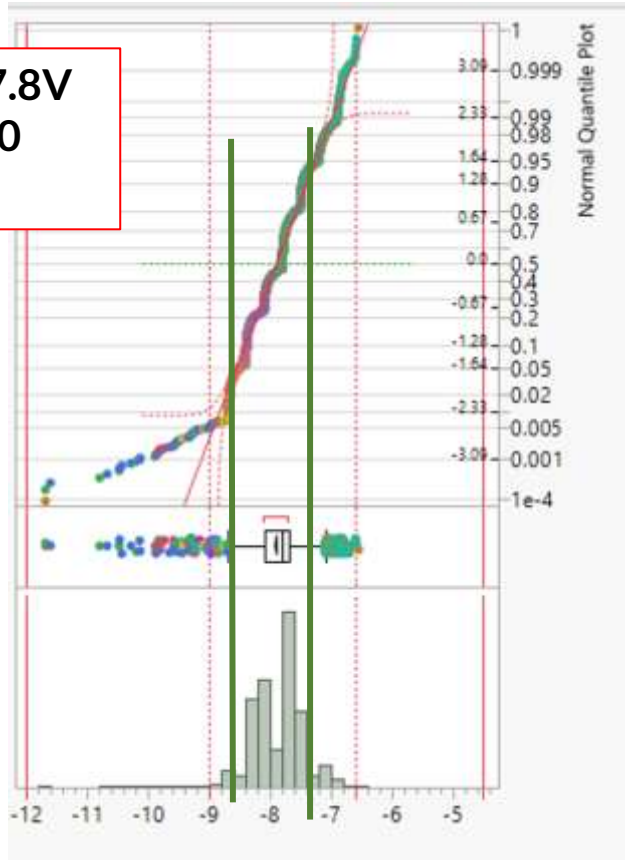
Paralleling of multiple devices: device consideration

measurement points





Median = -7.8V
Sigma = 0.40
N = 11063

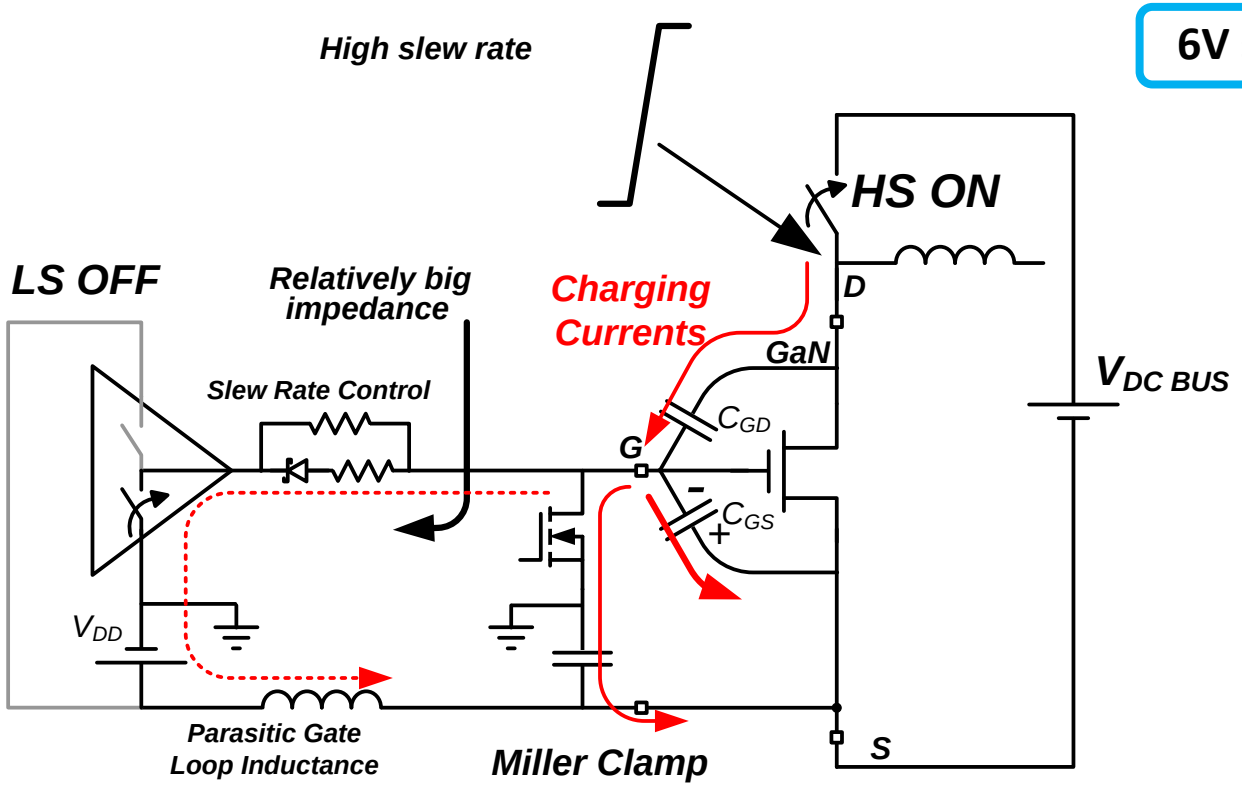


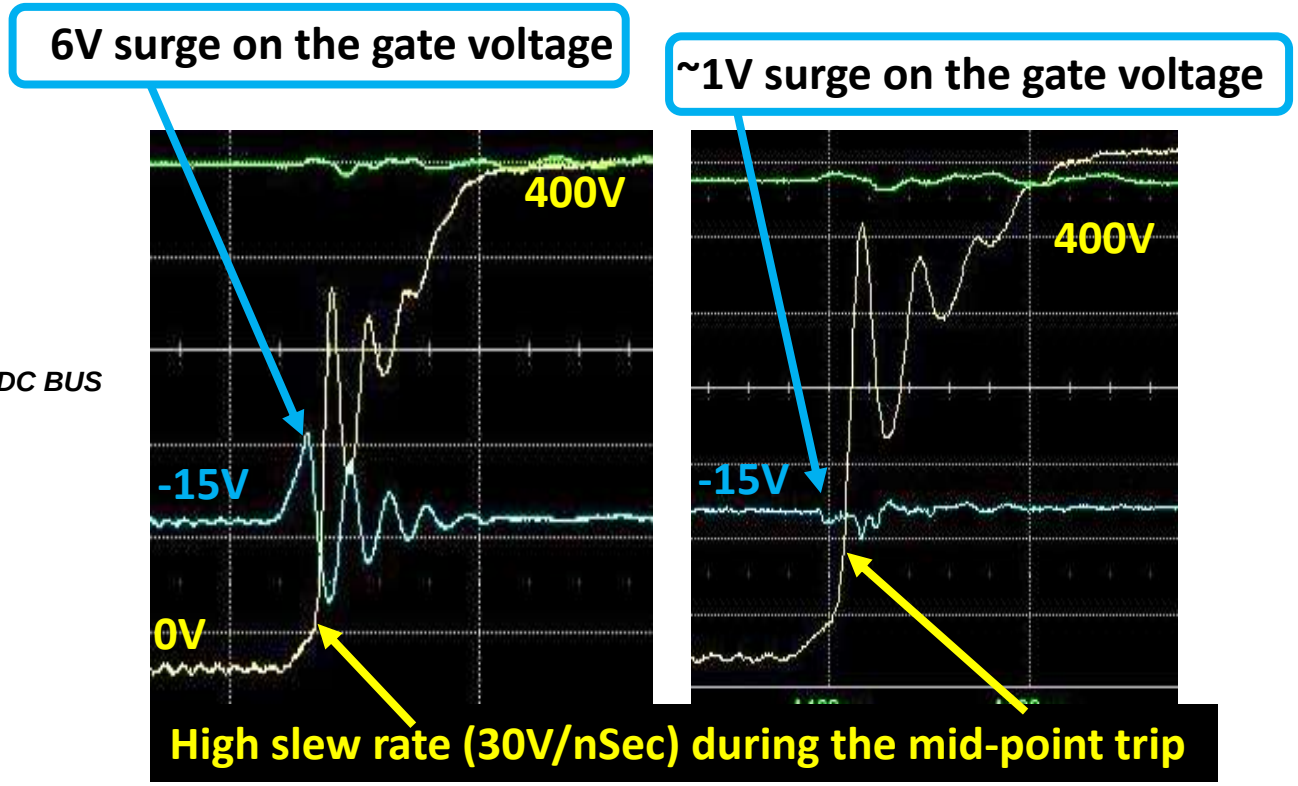
80% of the all devices are good to be assembled in the same module

Verification of current sharing by direct measurement of voltage waveform on inductance of Q2

→ Binning of devices by threshold voltage with “bin” size of +/- 0.5V

Parasitic signals & spikes control by Miller clamp





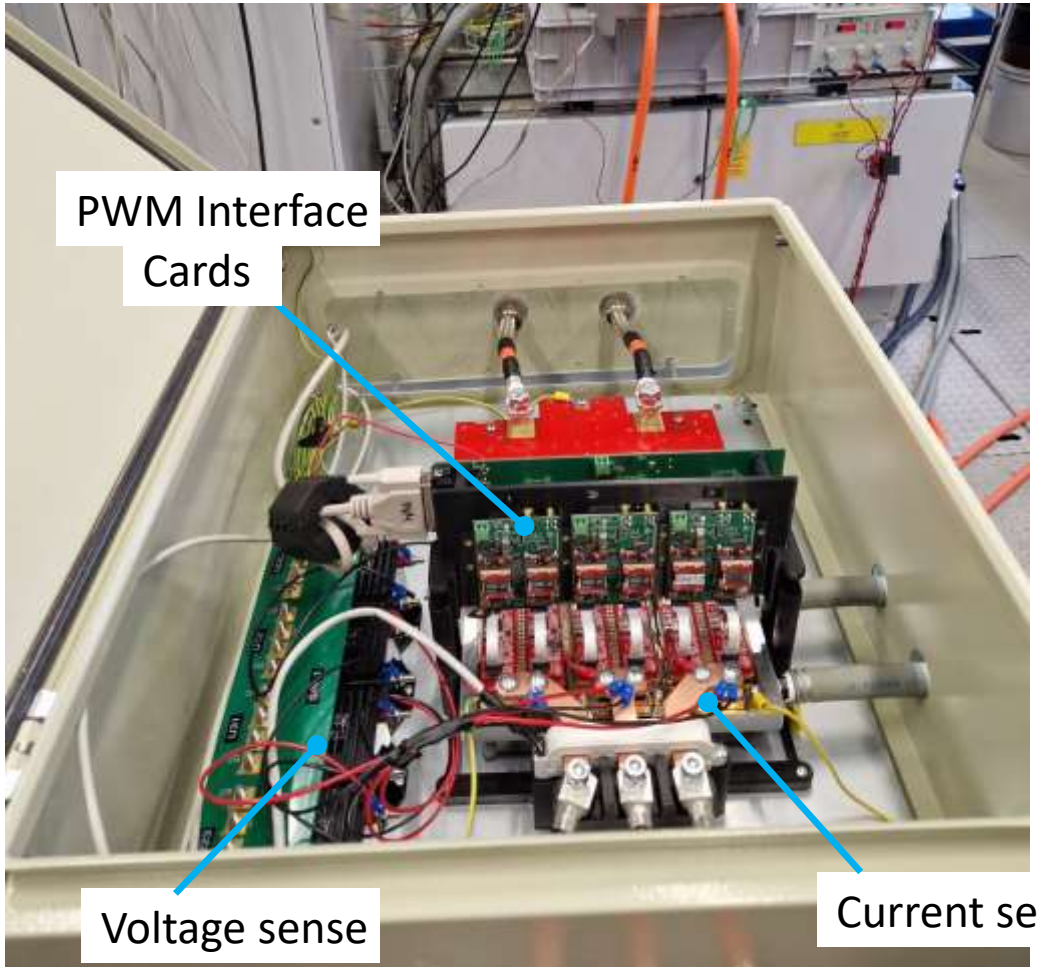
The “turn off” clamping through the driver is not efficient due to impedance of the slew rate control circuit and gate loop inductance. A proper layout and synchronization of “Miller clamp” are essential to hold switch OFF during the trip of the mid point. The gate surge can be reduced to couple of volts. High slew rate of **30 V/ns** does not change.

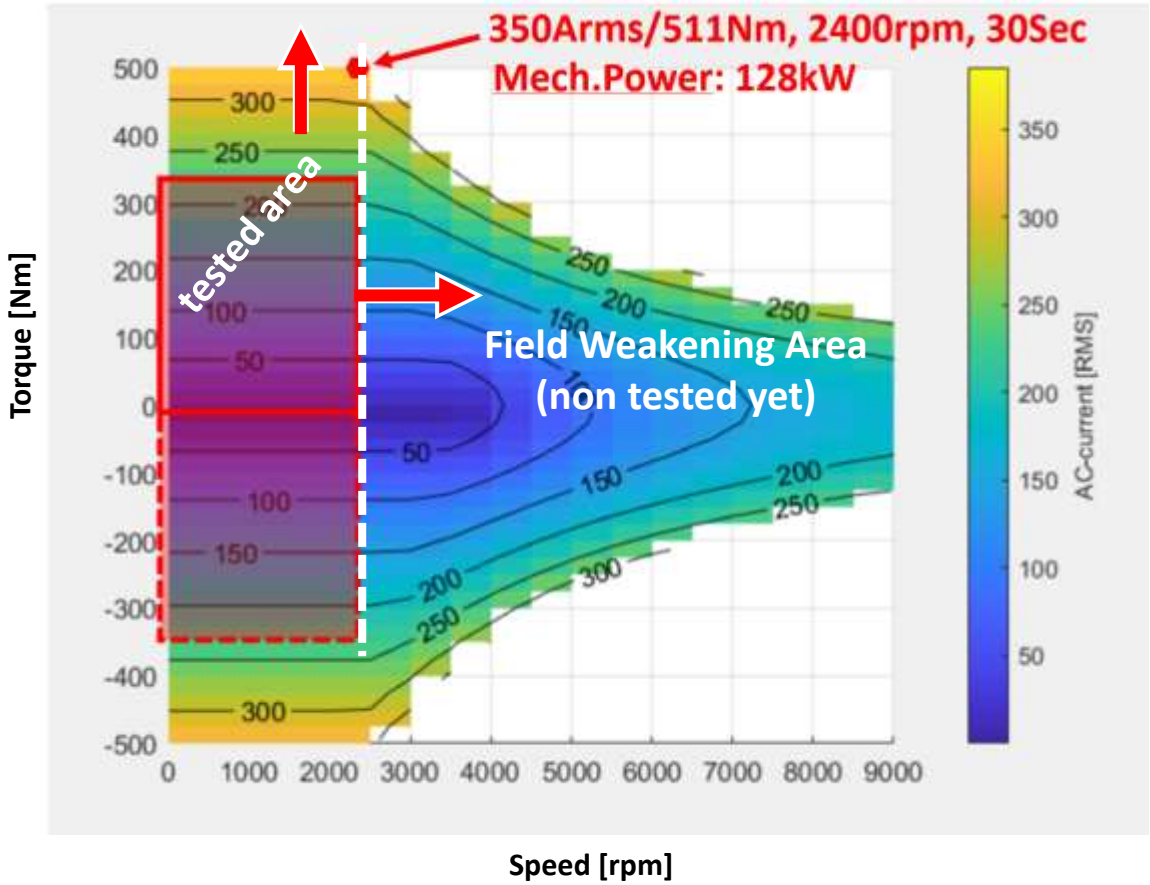
Suppression of oscillation in GaN reverse conduction

- GaN does not have body diode →
  - Reverse conductivity is through the same channel →
    - GaN has high transconductance and positive feedback in reverse conductivity → result in oscillations
- As a result, traditional capacitance Miller ratio optimization (Cgs >> Cgd) does not work, and tuning must be done per specific design with external Cgs capacitance

Results: 400V EV GaN based prototype

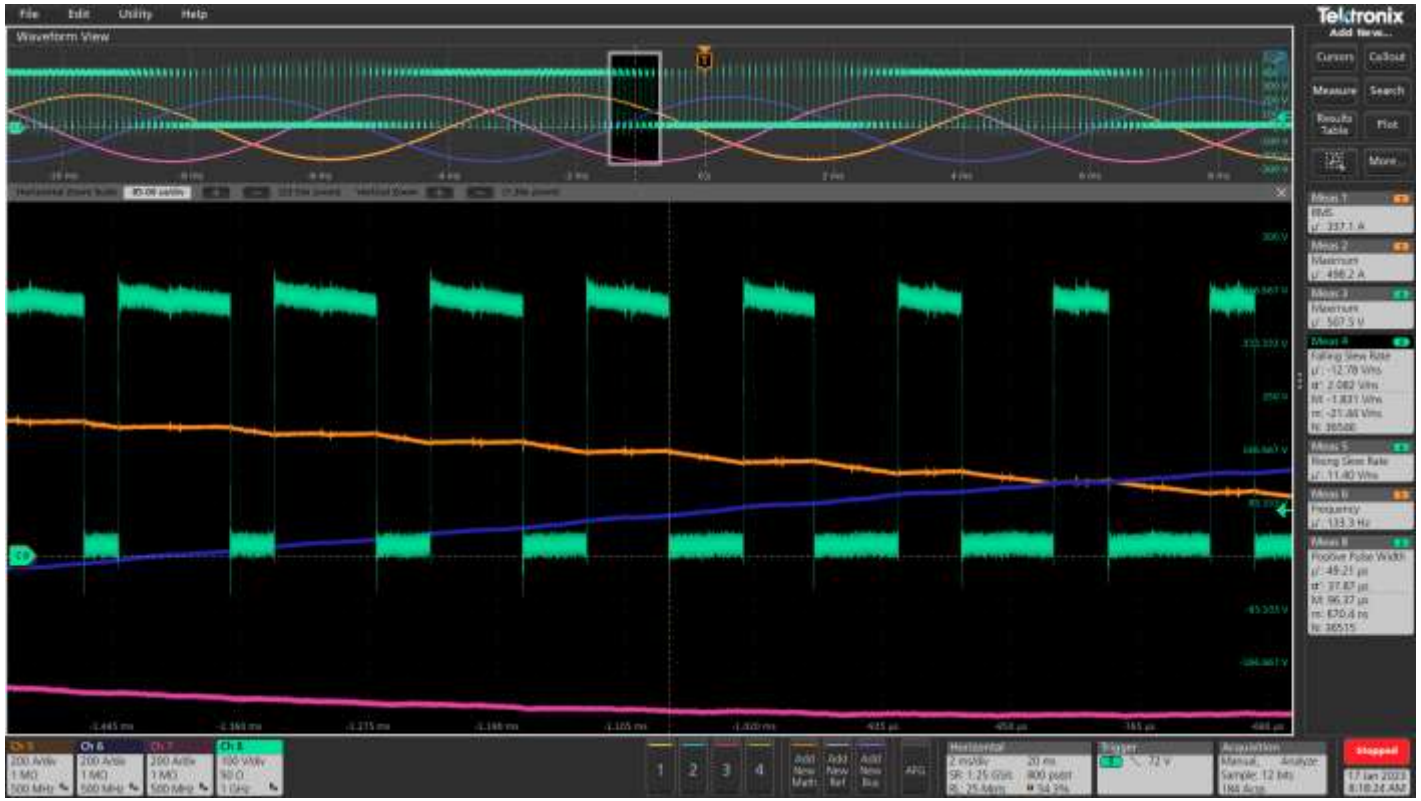
3-Phase GaN Inverter , Closed loop DYNO set up, tested up to 113 kW





Results: 400V EV GaN based prototype ,

400VDC ; Phase current 350Arms/500Apeak;
Velocity 2400 rpm



Wave forms of phase voltage and currents of inverter output

navy – phase 2 voltage; orange – phase 1 current
blue – phase 2 current; magenta – phase 3 current

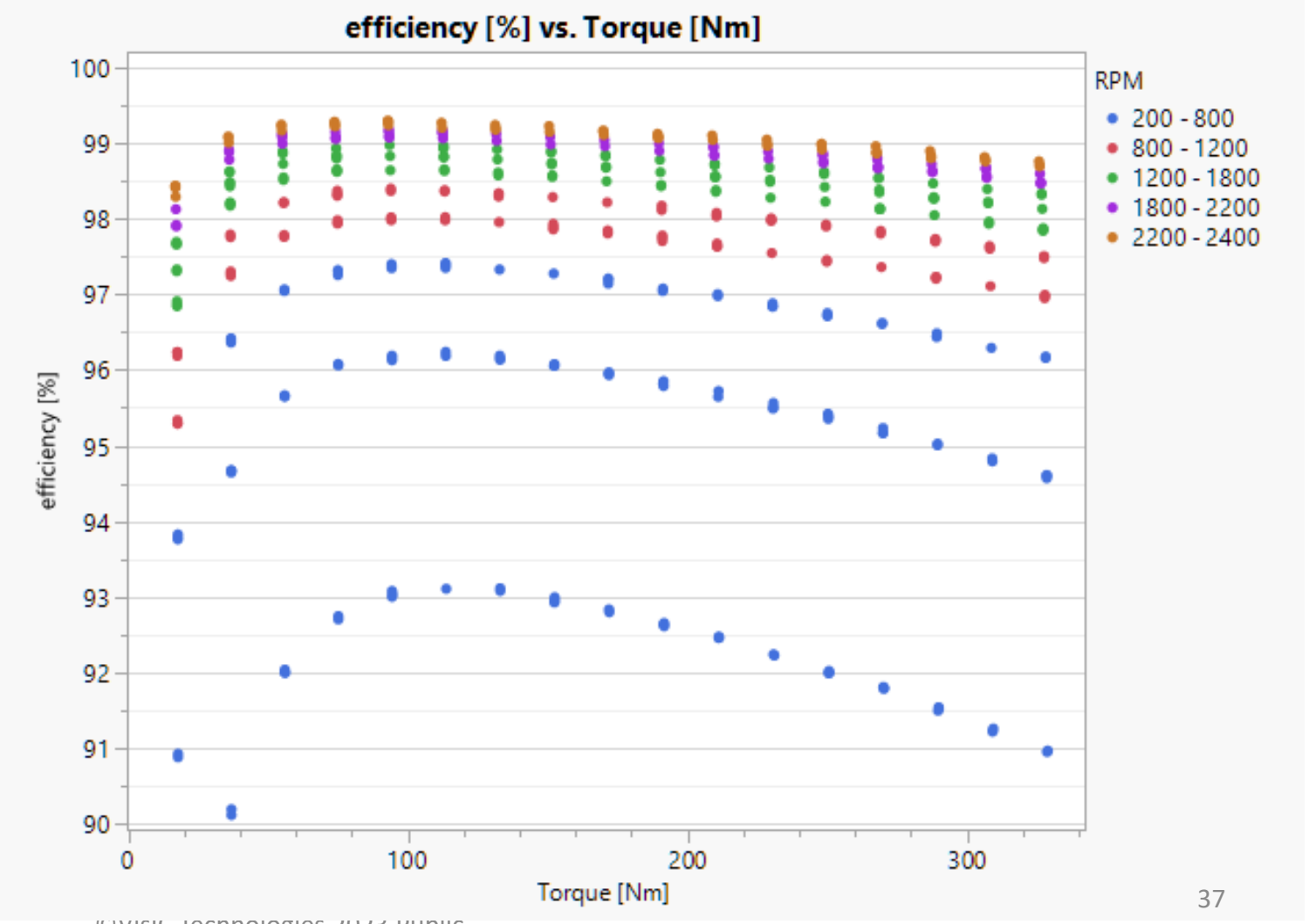
Sum of "phase" power is "output" power of the inverter

Input power of the inverter

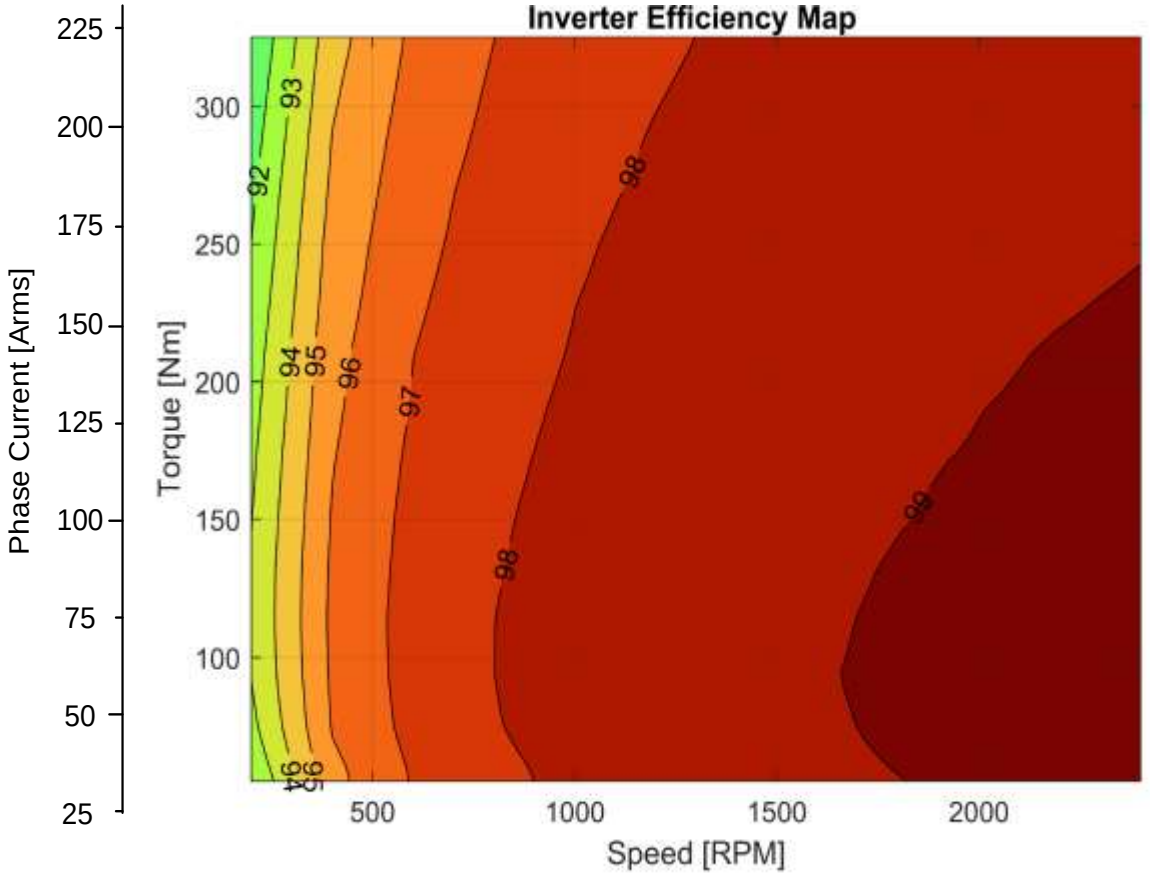
Results of power meter:
- Element 1/2/3 is measurements of phases 1, 2, 3 correspondingly,
- Element 4 – is measurement of the inverter input

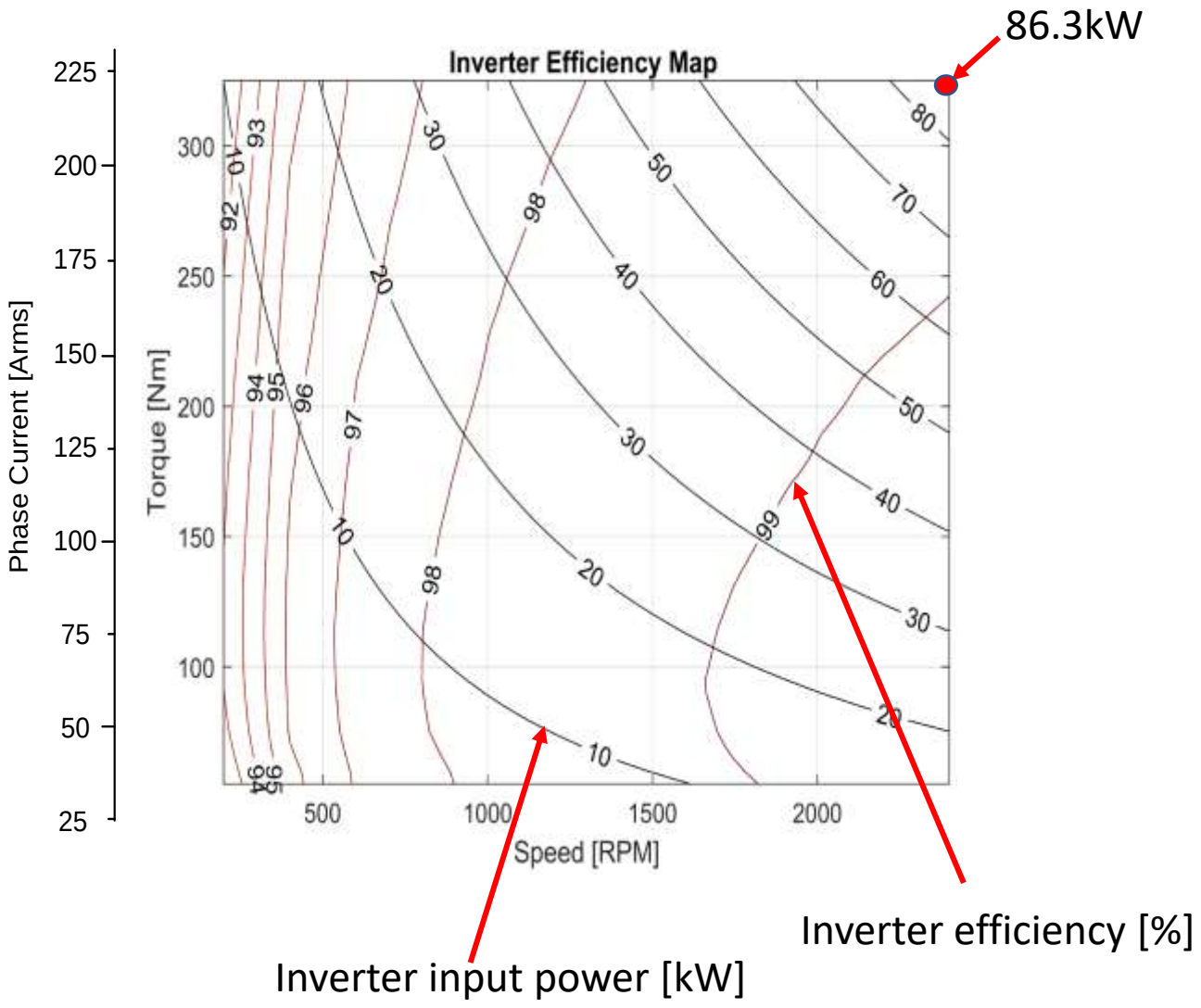
WLTP Driving Cycle Efficiency

- Max Efficiency point:
  - **99.295%**
  - 2400RPM (160Hz)
  - 92.8NM
  - 24.4KW output



WLTP Driving Cycle Efficiency



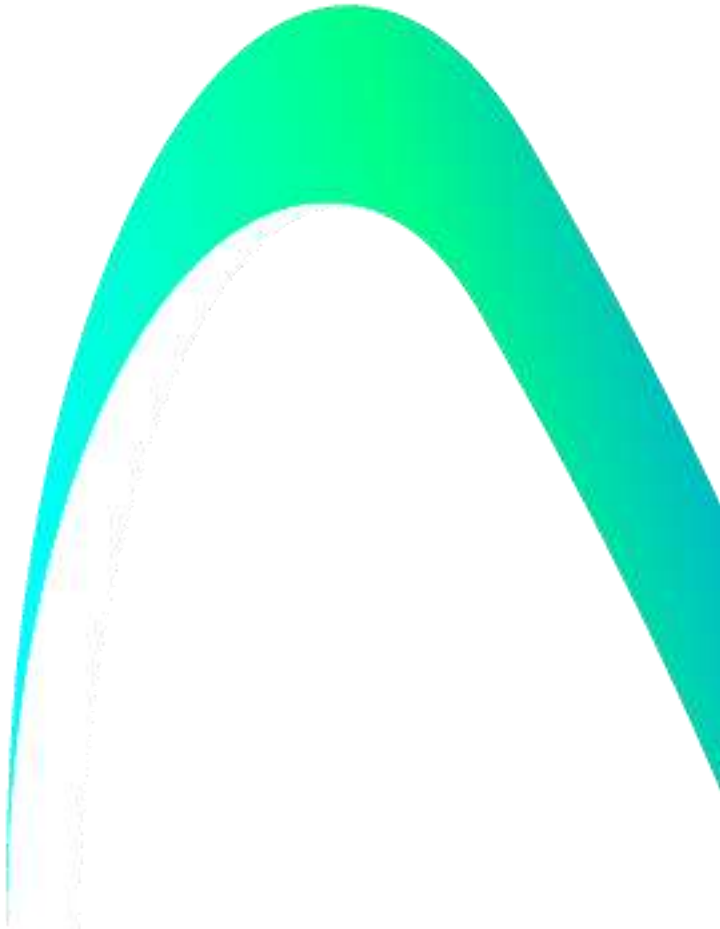


Switching frequency 20kHz

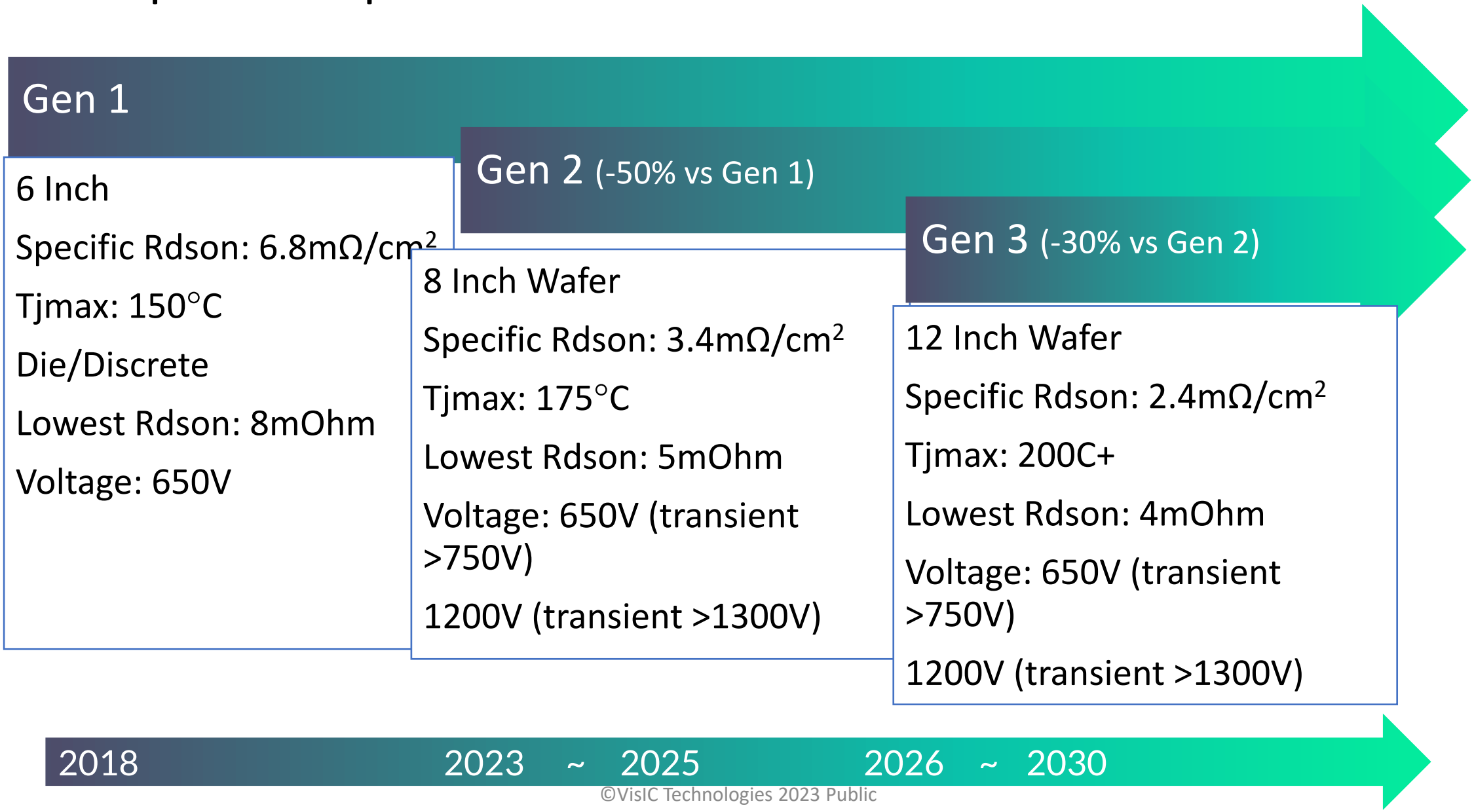
Type of modulation Space Vector Modulation

Summary and

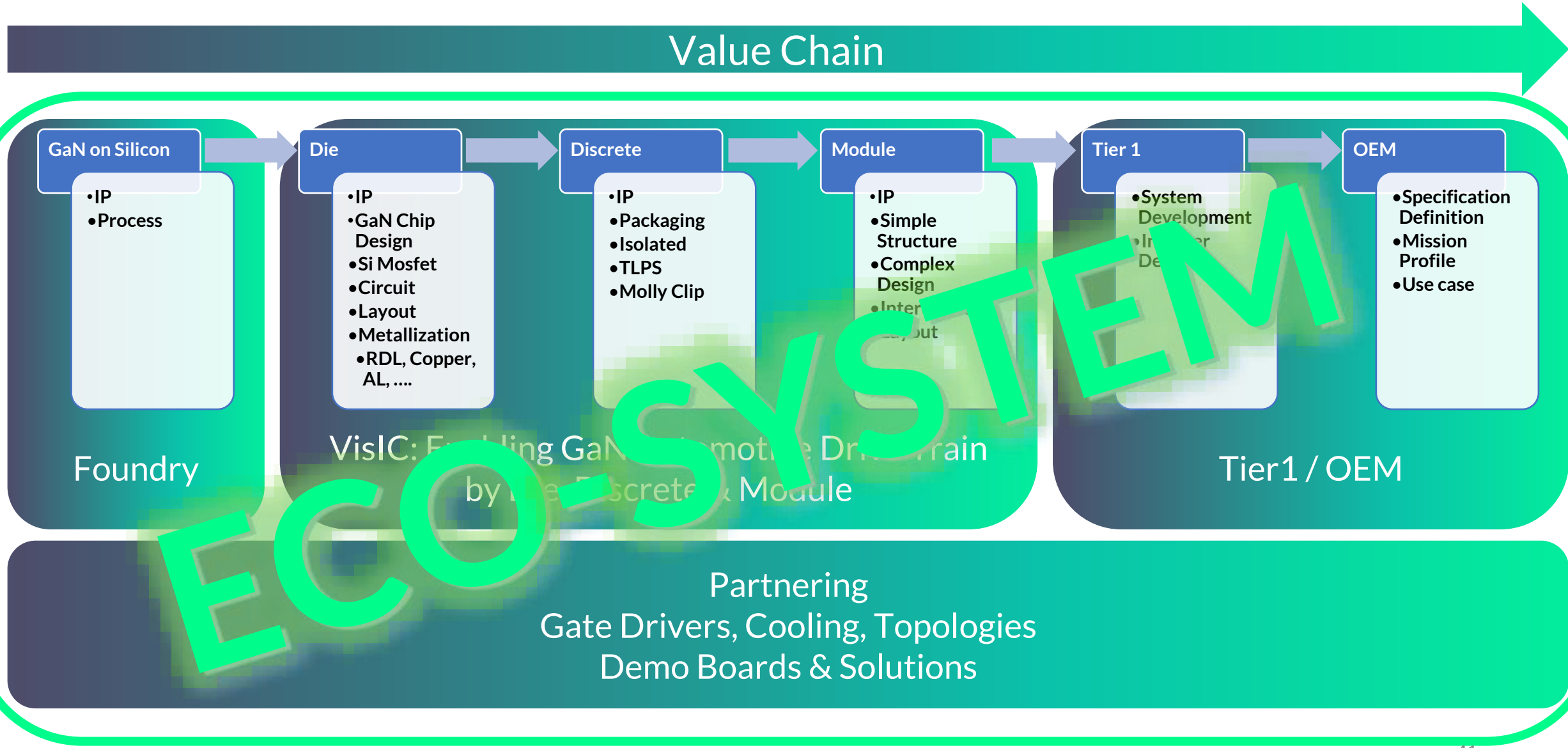
What is next?



More power packed in GaN



VisIC Value Chain

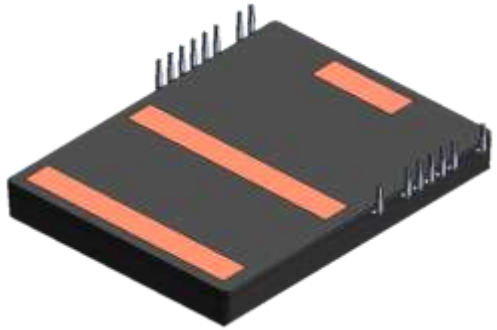


GaN modules and embedding systems will emerge

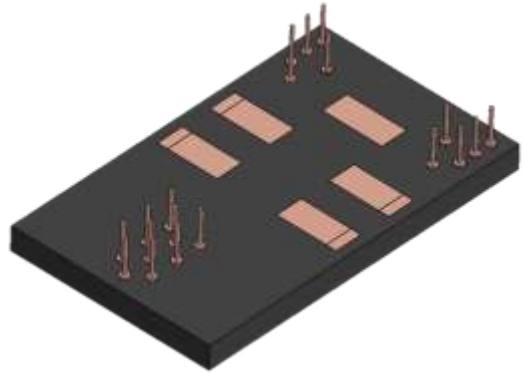
VisIC GaN Module Design

Gen 1 → 2

VM022
Prototype based on
4 parallel discrete
V08 SMD



VM044
A-Sample based on
2x parallel V08 die



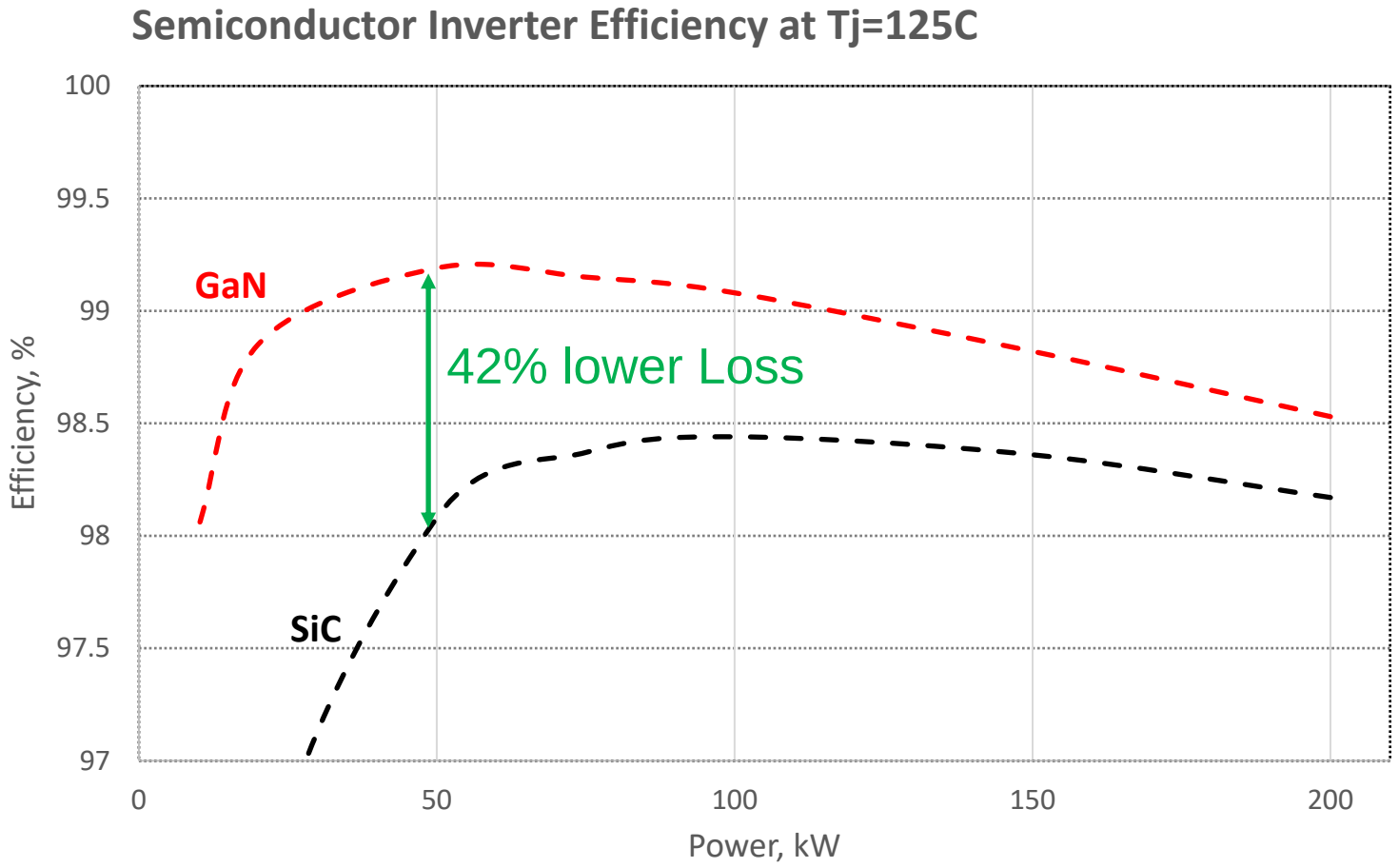
VM027 V2

High Voltage Power Reliability

What is next: 800V

200kW GaN Inverter Simulation

- **GaN Three-level* compared to Two-level SiC based on Cree CAB400M12XM3**

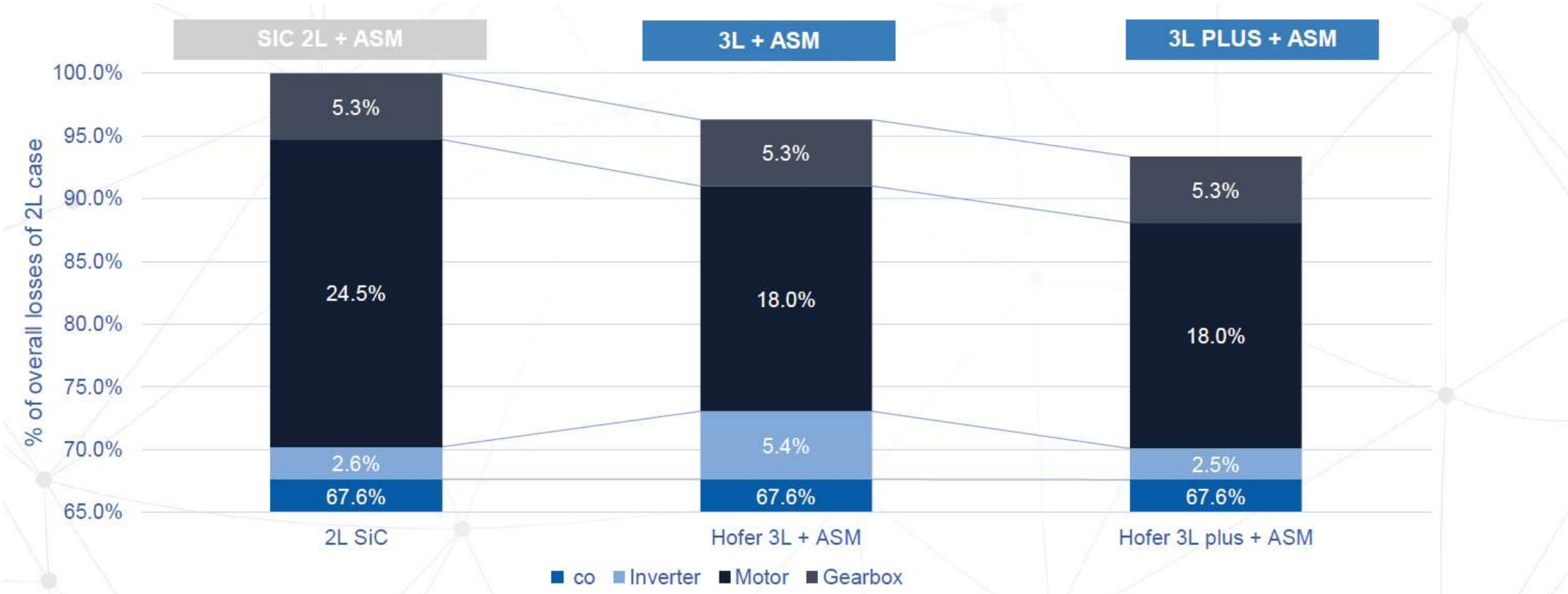


3 level GaN solution shows **a visible cost/performance advantage** versus SiC 2 level

*Based on Flying Capacitor Topology using next generation GaN device with reduced Rdson

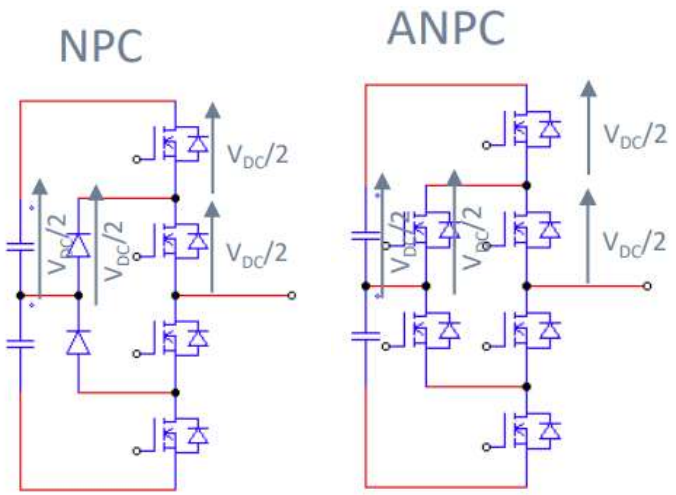
WLTC System Impact Comparison

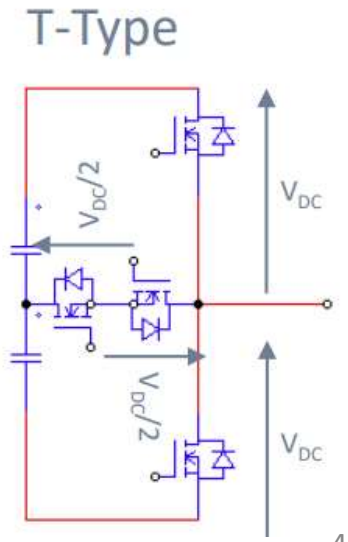
VisIC GaN devices



3L Topologies – GaN

Topology Criteria	NPC GaN 650V SiC Diode 650V	T-Type SiC Mosfet 1200V GaN 650V	ANPC GAN 650V
Efficiency	+	++	++
Footprint	+	++	-
Cost	+	--	+
Simplicity	+	++	-
Sustainability	+	-	++
Gate Driver	4x	4x	6x





	2L Si	2L SiC	2L GaN	NPC	TNPC	ANPC
η map	93.7%	97.4%	97.2%	97.4%	97.5%	97.6%
η drive	83.0%	94.1%	93.3%	94.4%	94.5%	94.0%

Tab. 1: Global TI efficiency. First line is the mean efficiency over the EM map. Second line is the mean efficiency over all driving cycles.

Source: Picture & Data - University of Bern

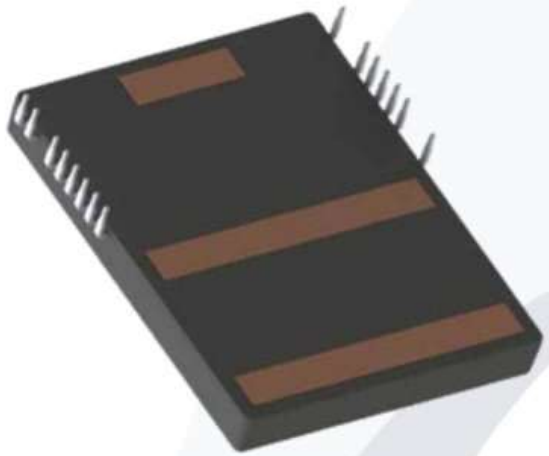
GaN power module oulook

4.4mΩ 650V Half-Bridge D³GaN™ Power Module

VM044HB065WT1TM11X00

Description

The Transfer Molded Half Bridge module integrates 8mΩ Power FETs for a 300A$_{rms}$ class inverter and can be paralleled for higher power.
The D³GaN™ technology uses high-density, lateral GaN power transistor, assembled into a Normally-Off product with extremely low $R_{DS(ON)}$ and exceptionally efficient switching performance.
The integrated safety functions ensure safe operation during system start up and shutdown, while having no impact on the switching performance of the GaN transistor.



Key Features

- Low inductance terminal connection to Busbars
- Weldable power terminals
- Thermal case designed for sintering to the heatsink
- High Threshold voltage for fast switching transients
- High performance SiN ceramic substrate
- Standard 15V gate drive voltage
- NTC sensor
- Package Size 50x38x6mm

Applications

- Hybrid and Electric Vehicle Traction Inverter
- High Power DC-DC Converter

	VM044
Power Loop	5.7nH
Miller Current Gate Loop	3nH
Size	50x38x6mm

VM044

2x V08/switch position

Sample Available Q3 2023

GaN can operate 400V EV inverter in passenger car power range

It is a lot of engineering work ahead to get GaN on the road in millions of EV

VisIC TECHNOLOGIES

THANK YOU