Feasibility Study of D3GaN Power Module for 2 Level 400V BEV Inverter

Dieter Liesabeths
SVP of Products

28. March 2023

Agenda

- VisIC Company introduction
- Comparison of different GaN technologies to D^3GaN
- Driver circuit
- Paralleling of D^3GaN Devices
- Short circuit protection scheme
- Case Study 400V 2L BEV Inverter
- Outlook on next Power Modules
- Summary

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Company Overview

Company Overview

- VisIC Technologies Ltd is a company established in 2010 under the laws of Israel
  - Wholly owned subsidiary in Shanghai 微思芯电子技术（上海）有限公司, established in 2020
  - Wholly owned subsidiary in Phoenix, AZ VisIC technologies LLC, customer support Packaging & Assembly, established in 2022
  - Wholly owned subsidiary in Vienna, Austria, finalizing setup
  - Agile supply chain as a fabless operation using

Locations

- Visic Technologies HQ
- VisIC Shanghai China Support
- VisIC Reliability & Qualification
- VisIC Munich Europe Sales
- VisIC Hsinchu Operation
- VisIC Sales APAC US
- VP OPS
- VisIC customer support,
- VisIC Europe App Center

VisIC Value Chain

Value Chain

GaN on Silicon
- IP
- Process

Die
- IP
- GaN Chip Design
- Si Mosfet
- Circuit
- Layout
- Metallization
  - RDL, Copper, AL, ….

Discrete
- IP
- Packaging
- Isolated
- TLPS
- Molly Clip

Module
- IP
- Simple Structure
- Complex Design
- Interc…
  Layout

Tier 1
- System Development
- In…
  De…

OEM
- Specification Definition
- Mission Profile
- Use case

Foundry

VisIC: Enabling GaN Automotive Drive Train by Die-Discrete & Module

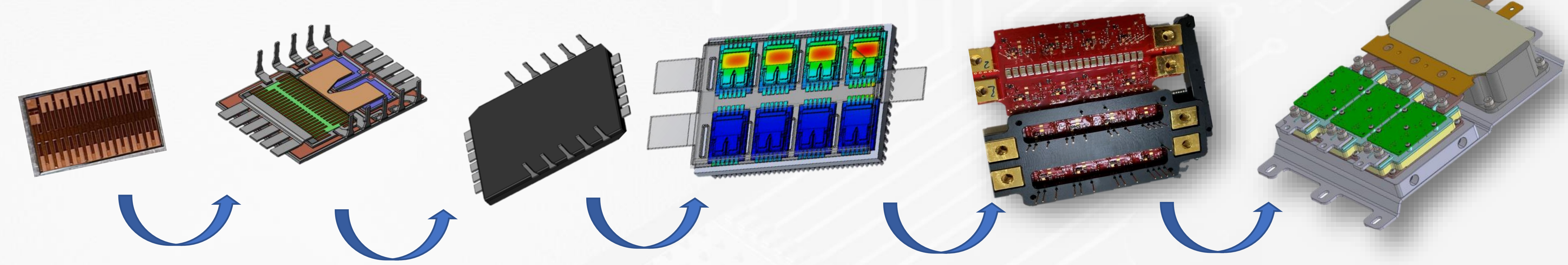
Tier1 / OEM

ECO-SYSTEM

Partnering
Gate Drivers, Cooling, Topologies
Demo Boards & Solutions

Die to Inverter Integration

- Technology vehicle: &00A HB module, open frame concept to speed up VisIC's and customer's learning curve



7 mOhm D-mode die
> 200A current capability

- Power board and control optimization process, high current (600A) testing,

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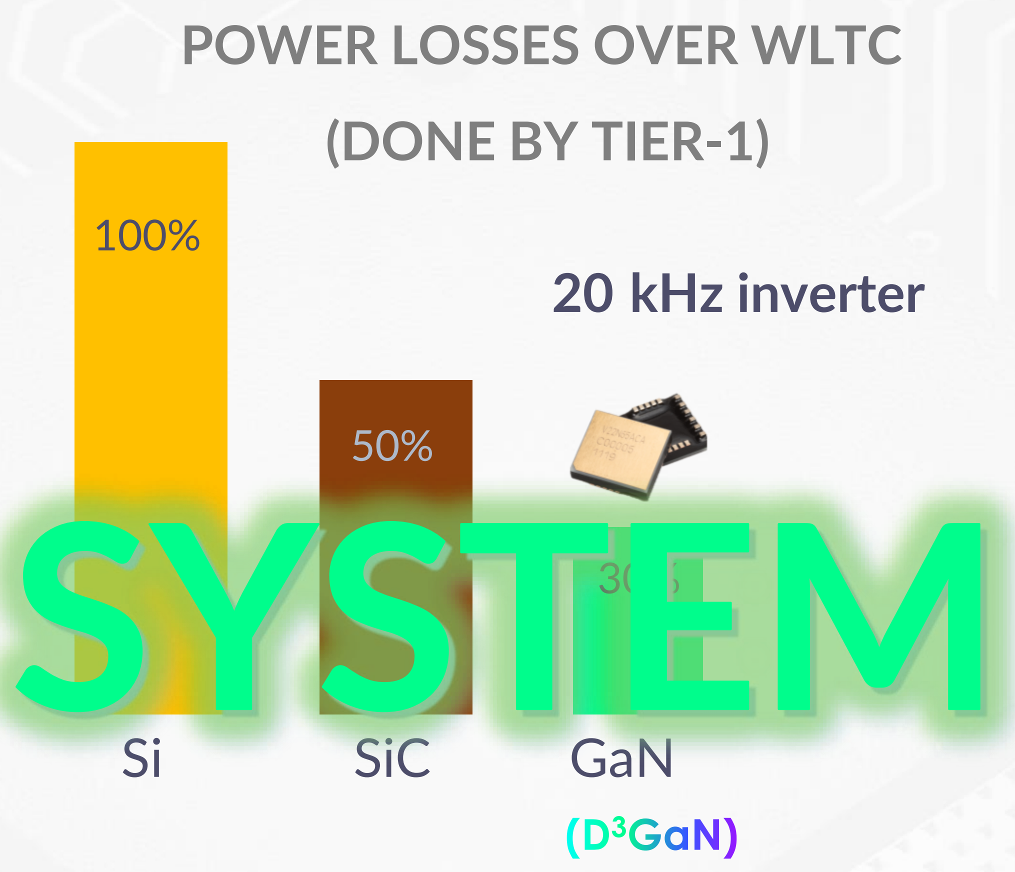
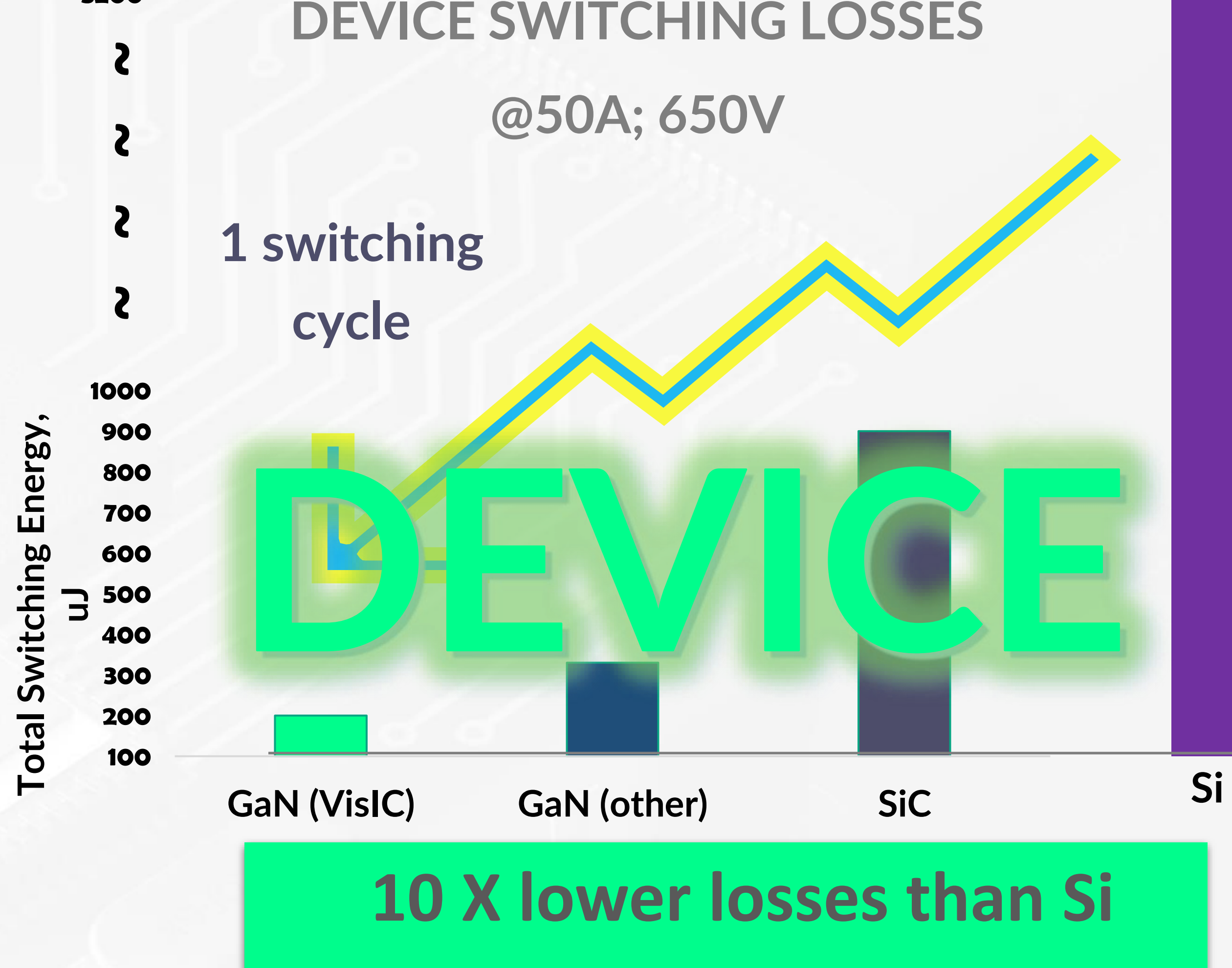
Fundamentals of Inverter Operation: Test data

ACTUAL TEST DATA





3 X lower losses than Si

2 X lower losses than SiC

10 X lower losses than Si

4.5 X lower losses than SiC

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Comparison of different GaN technologies

D^3GaN vs Other GaN

MISHEMT D-mode

D^3GaN

Texas Instruments

Cascode: Transphorm, Nexperia

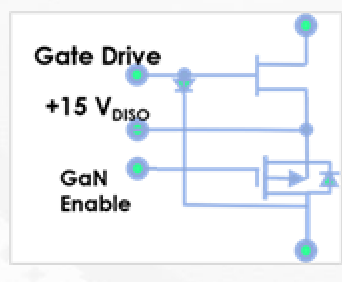
JFET or MIS HEMT

E-mode TSMC, Panasonic (Infineon)

D^3GaN (VisIC)

ADVANTAGES
- Low switching loss
- Robust Positive V_{TH}
- Low R_{ON}
- Easy paralleling
- Standard Si driver 0/+15

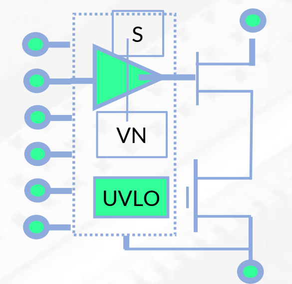
CONCERNS
- Package complexity



Texas Instruments

ADVANTAGES
-Low switching loss
-Driver integration with full protection

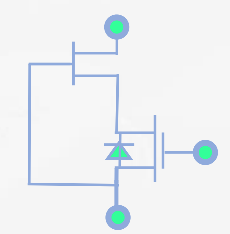
CONCERNS
-Low Power dissipation
-Complex paralleling
-Package complexity



Cascode: Transphorm, Nexperia

ADVANTAGES
- Standard Si driver
-Robust Positive VTH

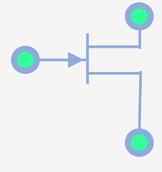
CONCERNS
-Complex paralleling
-Package complexity
-High LS inductance
-High switching losses



JFET or MIS HEMT

ADVANTAGES
- Easy paralleling
-Single die solution

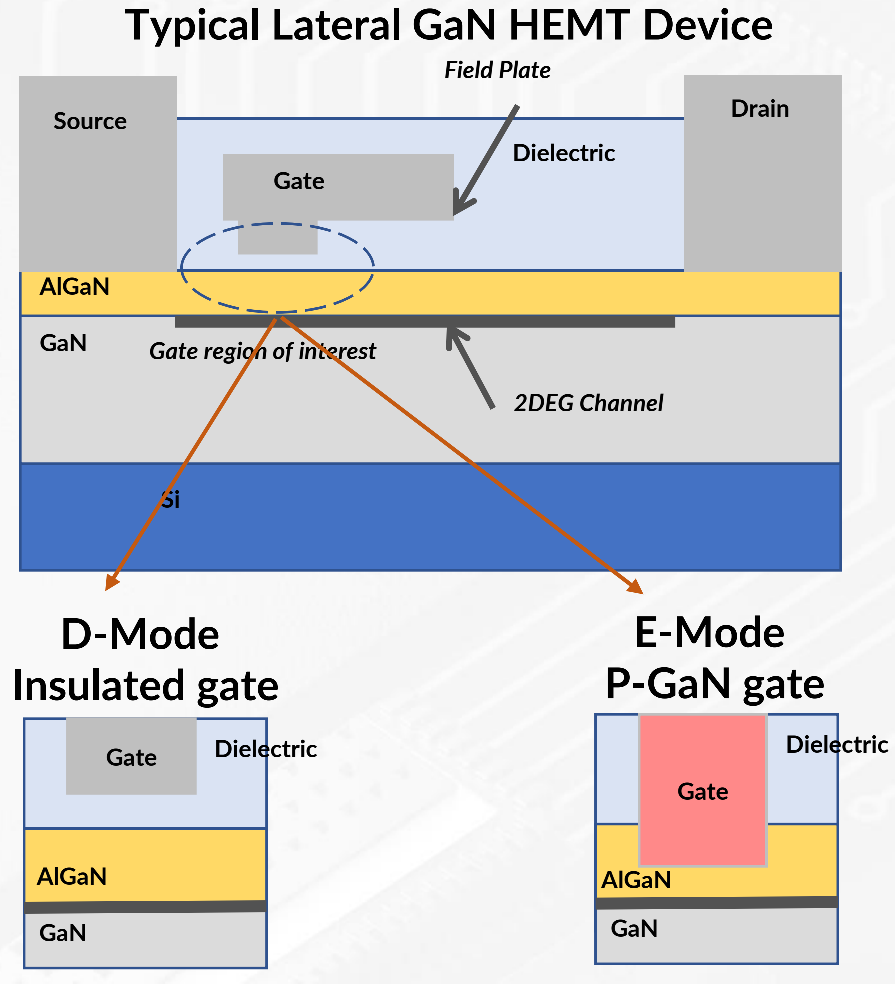
CONCERNS
-Low VTH
-Low gate isolation



D-mode vs E-mode GaN

Depletion mode (d-mode)

- Normally on device
- **Advantages**
  - **Large negative threshold voltage**
  - **Gate reliability not a concern**
  - **Standard gate drivers can be used**
- Disadvantages
  - Must have circuitry to be normally off
  - Uses cheap and reliable Si solutions



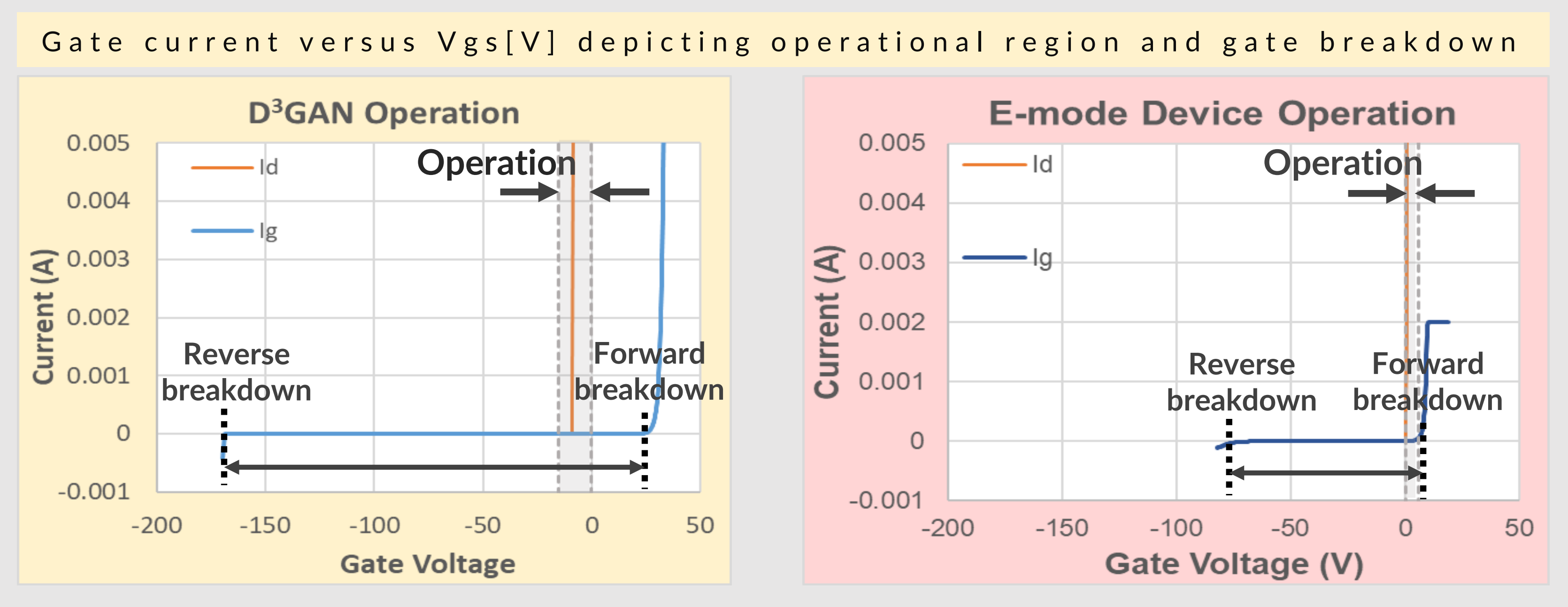
Enhancement Mode (e-mode)

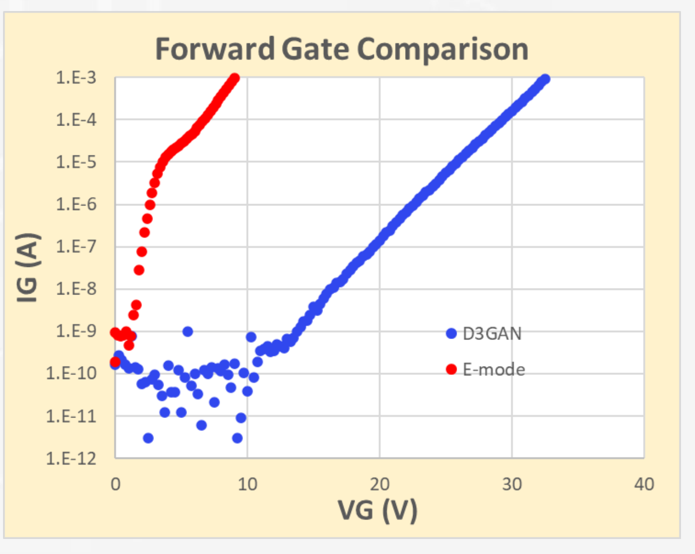
- Normally off device
- Advantages
  - Single chip solution
- Disadvantages
  - Small margin to positive gate overvoltage
  - Gate dielectric is critical
  - Specialized gate drivers needed
  - Sensitive to threshold voltage shift

D-mode provides easier path to product adoption in high reliability applications

D-mode vs E-mode GaN

- D-mode is proven reliable technology widely employed in RADARs front end
- D-mode has fundamentally lower specific RDSON for same class, due to absence of VT and RDRSON trade off
- D-mode has fundamentally better reliability and robustness due to absence of doping-introduced defects





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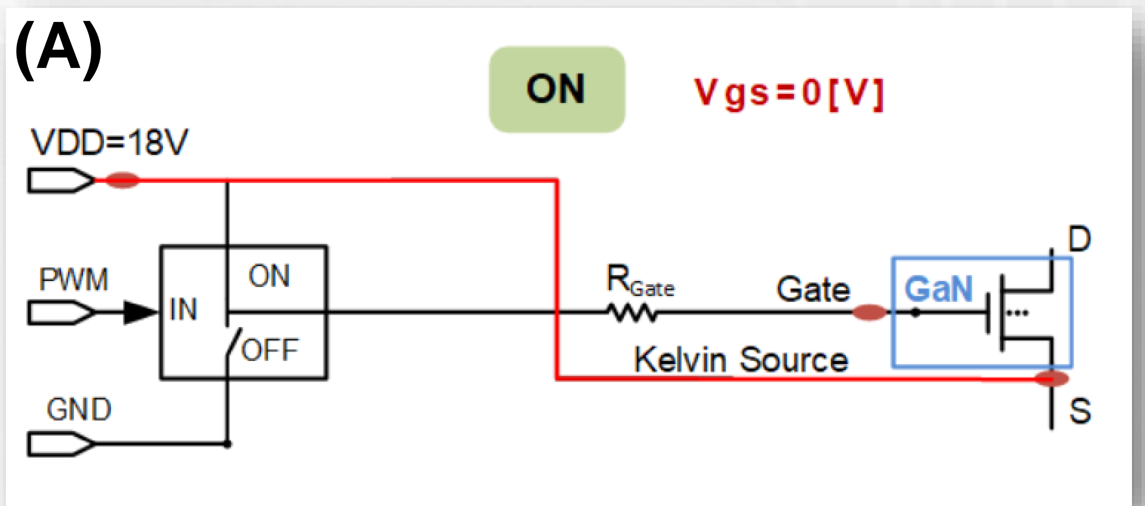
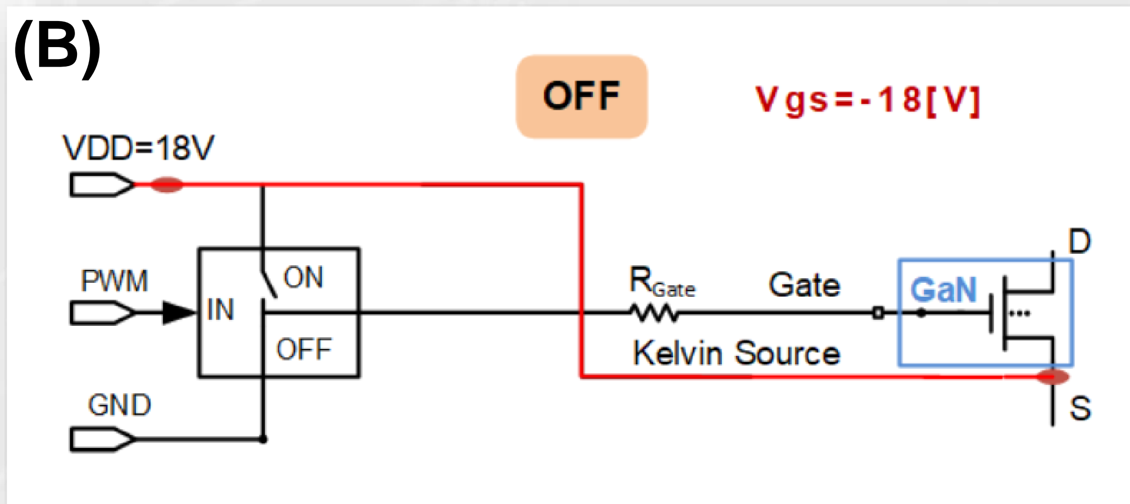
Driver Circuit

D3GaN – Direct Drive D-Mode GaN (1of2)

Gate – Source potential difference [Vgs] equals the difference of driver output potential and driver (VDD) potential.





Threshold voltage of GaN is -8V, therefore when

- Gate to Kelvin potential is 0V, GaN device is conducting (**A**)
- Gate to Kelvin potential is -18V, GaN device is not conducting (**B**)

Effective Threshold Voltage is +10V

As SiC, D3GaN uses standard of-the-shelf gate drivers with a standard of-the-shelf Auxiliary Power Supply (VDD)

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D3GaN – Direct Drive D-Mode GaN (2of2)

NOT A CLASSIC CASCODE

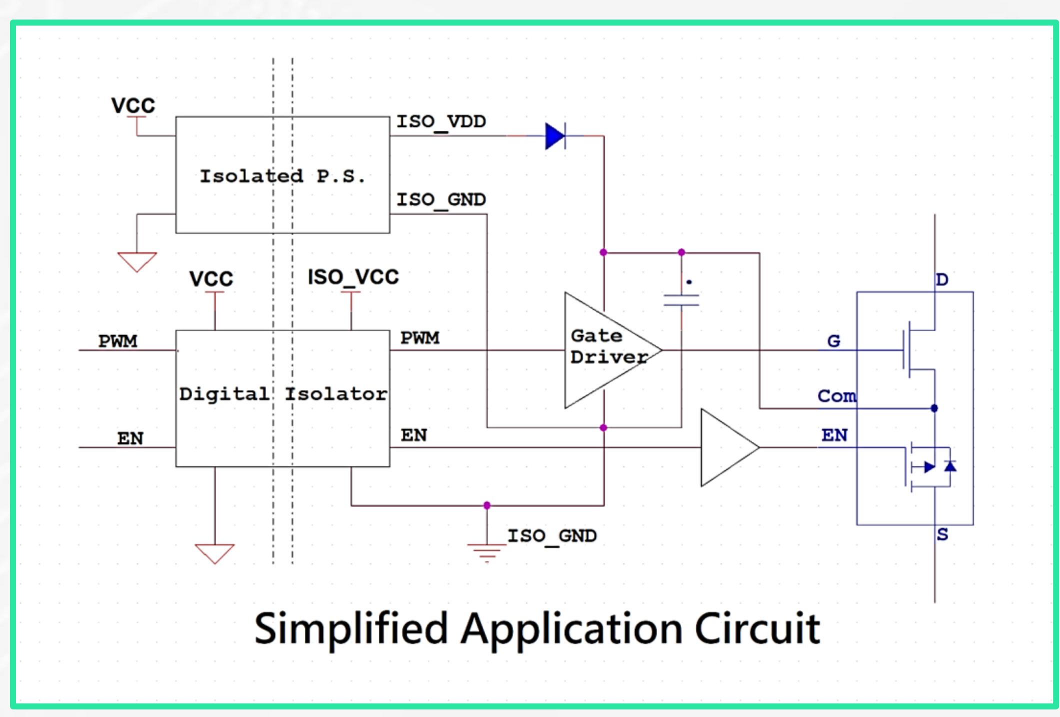
Q2 is ON when VDD is present and OFF when VDD is absent.

Q2 is not taking part in the switching process. It's held at "ON" during the switching of the D3GaN device

Gate Drive D3GaN

D3GaN Operation description

- HV bias is applied to Drain-Source -> as Q2 is normally OFF, voltage rises on its Source. This induces negative Gate-Source potential on the GaN Gate, which is clamped to Drain of Q2 through Diode D1. When the negative GaN Gate-Source potential reaches the its threshold voltage of -8V it is turned off (in a similar fashion to a Cascode operation).
- HV bias is applied to Drain-Source and all control Pins are connected to the related pins of external driver IC, which is in power-off state without supplying of VDD. As Q3 in its OFF state the scheme operates as in case 1 preventing high current path to the driver.
- During normal device operation Q2 and Q3 are always in ON state -> GaN is driven directly from the driver and Q2 can be considered as a very small resistance.



Simplified Application Circuit

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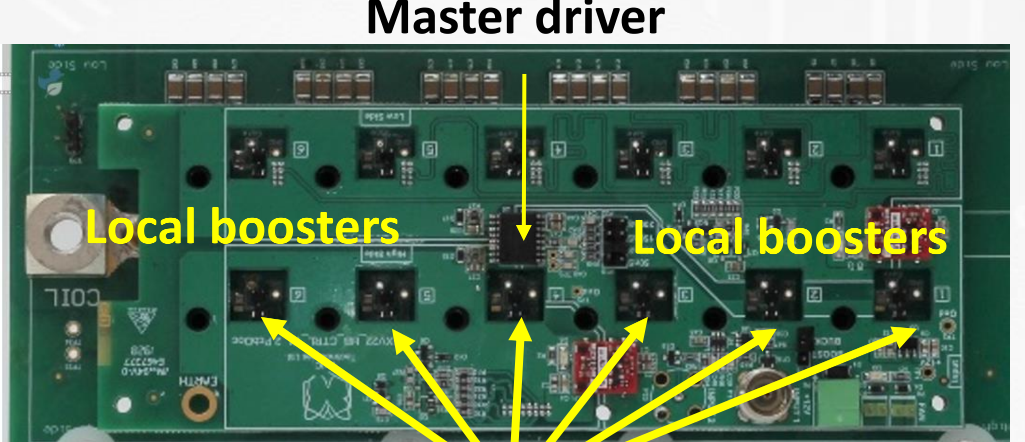
Paralleling of Devices

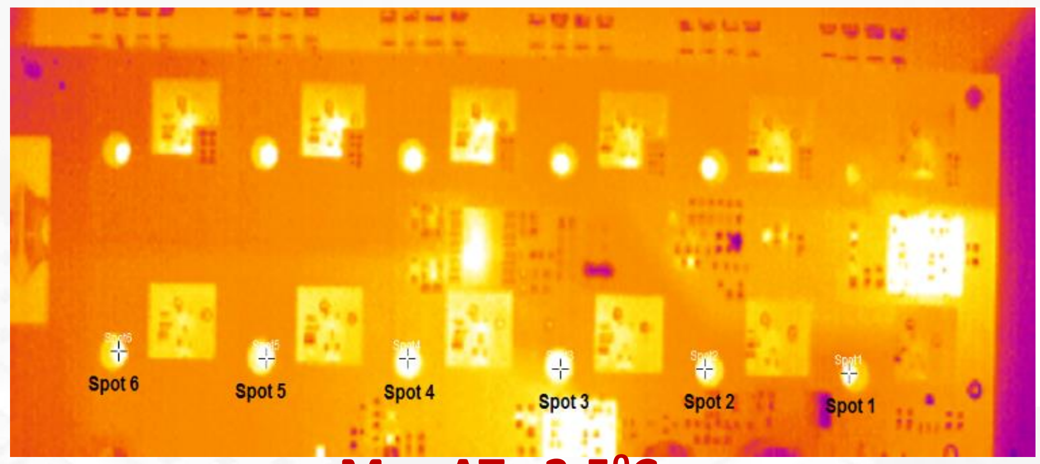
Paralleling of multiple devices: driver consideration

Use one Master and few boosters

Master driver



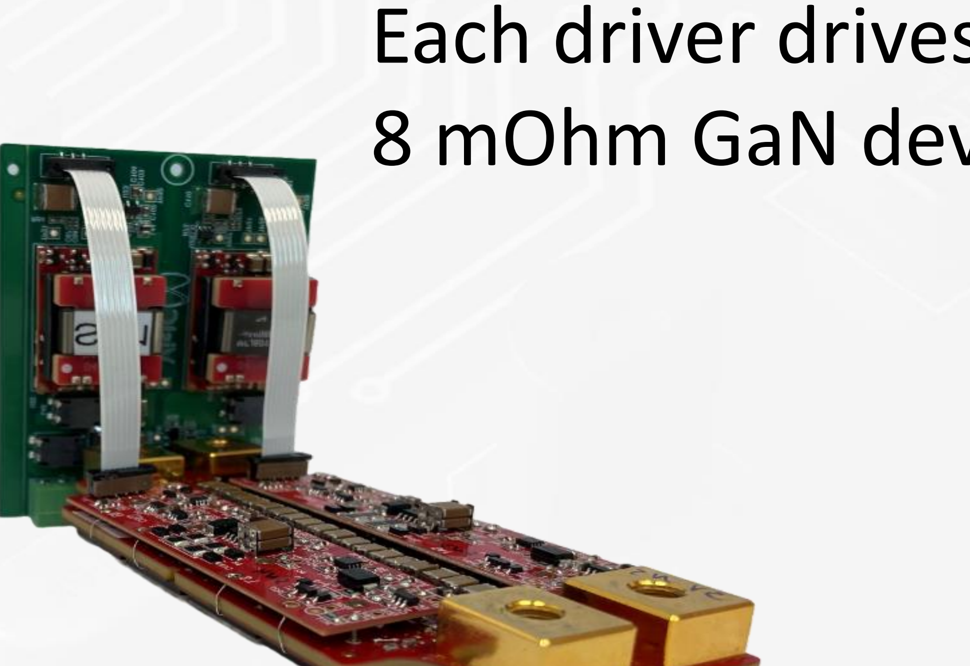
Local boosters



Max ΔT =3.5^{0}C

Use a two matched power driver chips in one package driver, e.g. 2ED24427 that has two 10 Amp matched drivers

Each driver drives two 8 mOhm GaN devices



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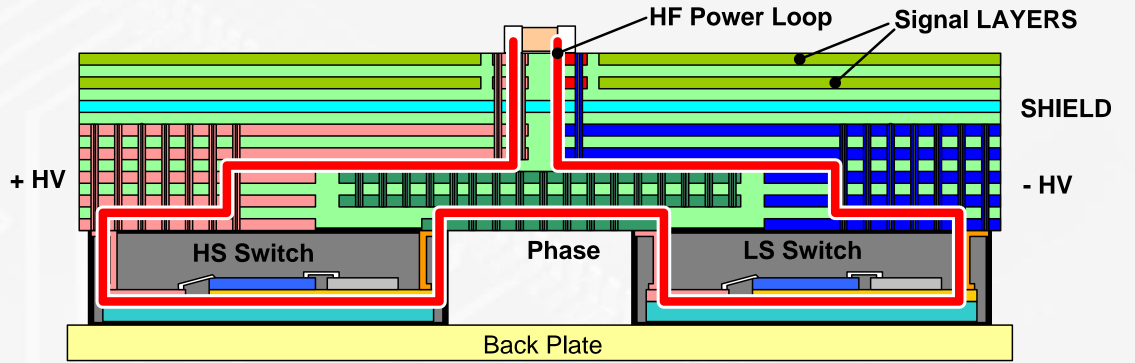
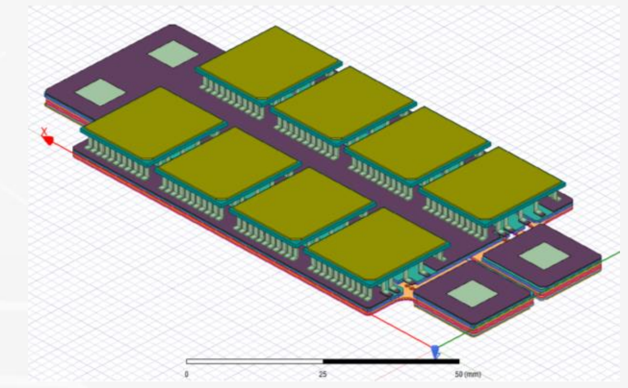
Paralleling of multiple devices: layout design

MAIN STEPS

1. Inductance reduction by minimizing the area enclosed by Power Loop
2. Increase current capability by adding layers and increasing Cu thickness
3. Decrease of capacitive coupling between phase terminal and rest of the circuit:
   by configuration of phase terminal
4. Reduction of HF noise coupling to control/driver circuits:
   by partitioning of functional areas, shielding



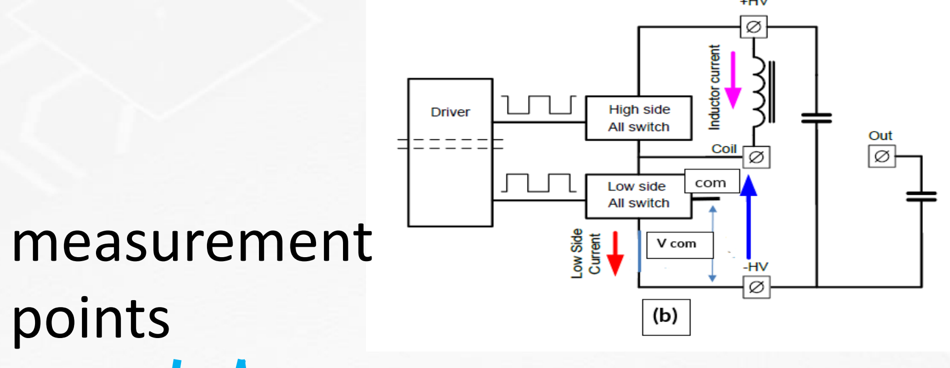
	Trace capacitance C[pF]		Stray Inductance L[nH]
	+HV'-Phase	-HV' -Phase	
VM022	235	240	1.87

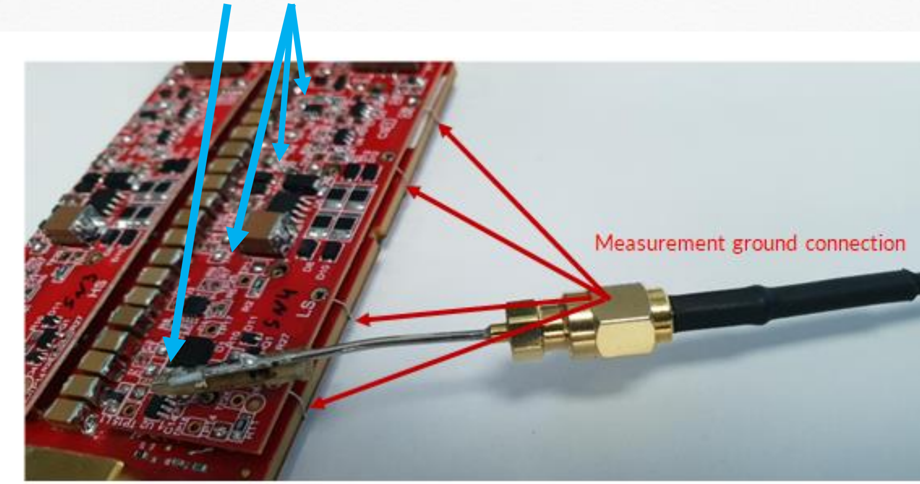


Paralleling of multiple devices: device consideration

VisIC TECHNOLOGIES

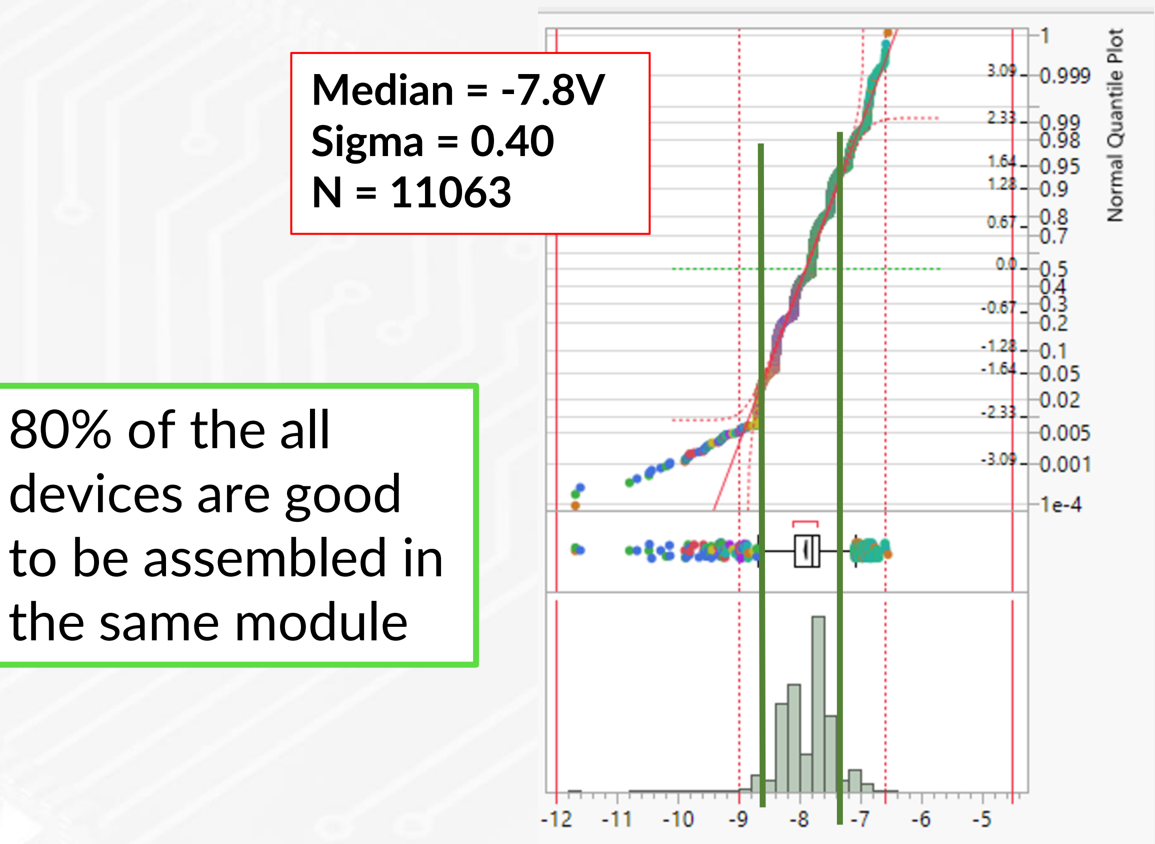
measurement points



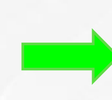


Median = -7.8V
Sigma = 0.40
N = 11063

80% of the all devices are good to be assembled in the same module



Verification of current sharing by direct measurement of voltage waveform on inductance of Q2



Binning of devices by threshold voltage with “bin” size of +/- 0.5V

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Short Circuit Protection Scheme

GaN HEMT Short Circuit Behavior

Measured Operation of V22

Idss

Hard Switching

Blocking Voltage

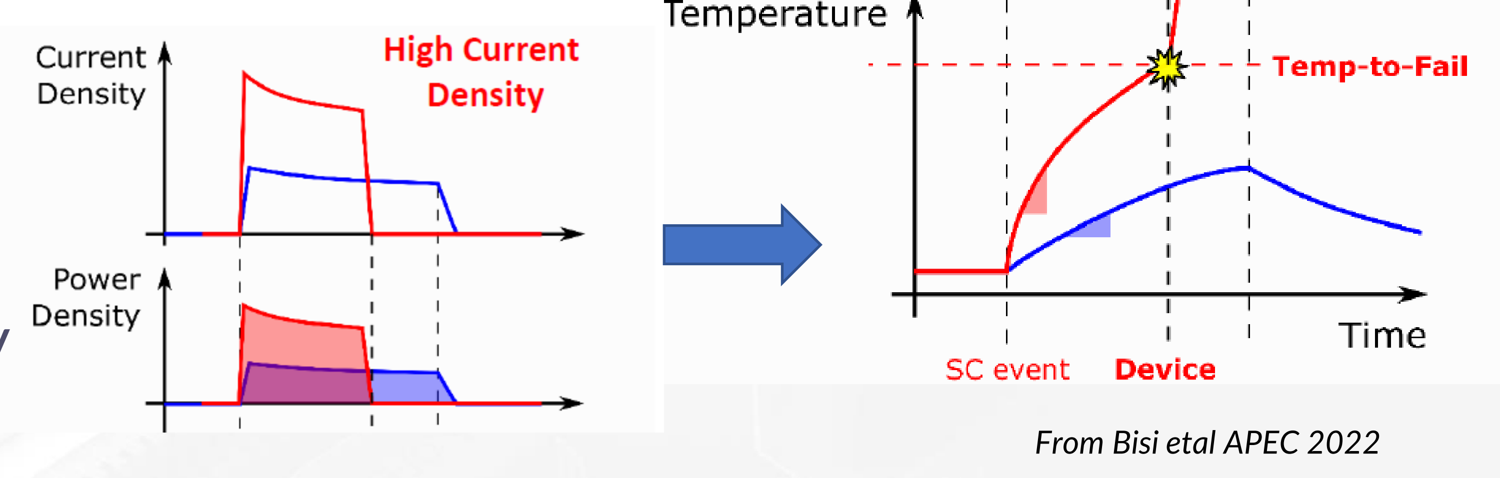
Id (A)

VD (V)

- GaN devices have very high saturation currents
  - **0.8 to 1.5 A/mm of gate periphery**
  - **More than 1kA for D³GAN devices**

- Power density rises rapidly with increasing current and exceeds the thermal capability of the device even at low voltages

- Saturation current does not reached
- Failure will occur in ~0.3 µsec
- Typical protection schemes rely on 1 to 2 µsec to respond to rising current



From Bisi etal APEC 2022

Lateral GaN devices require different approach to surge current protection

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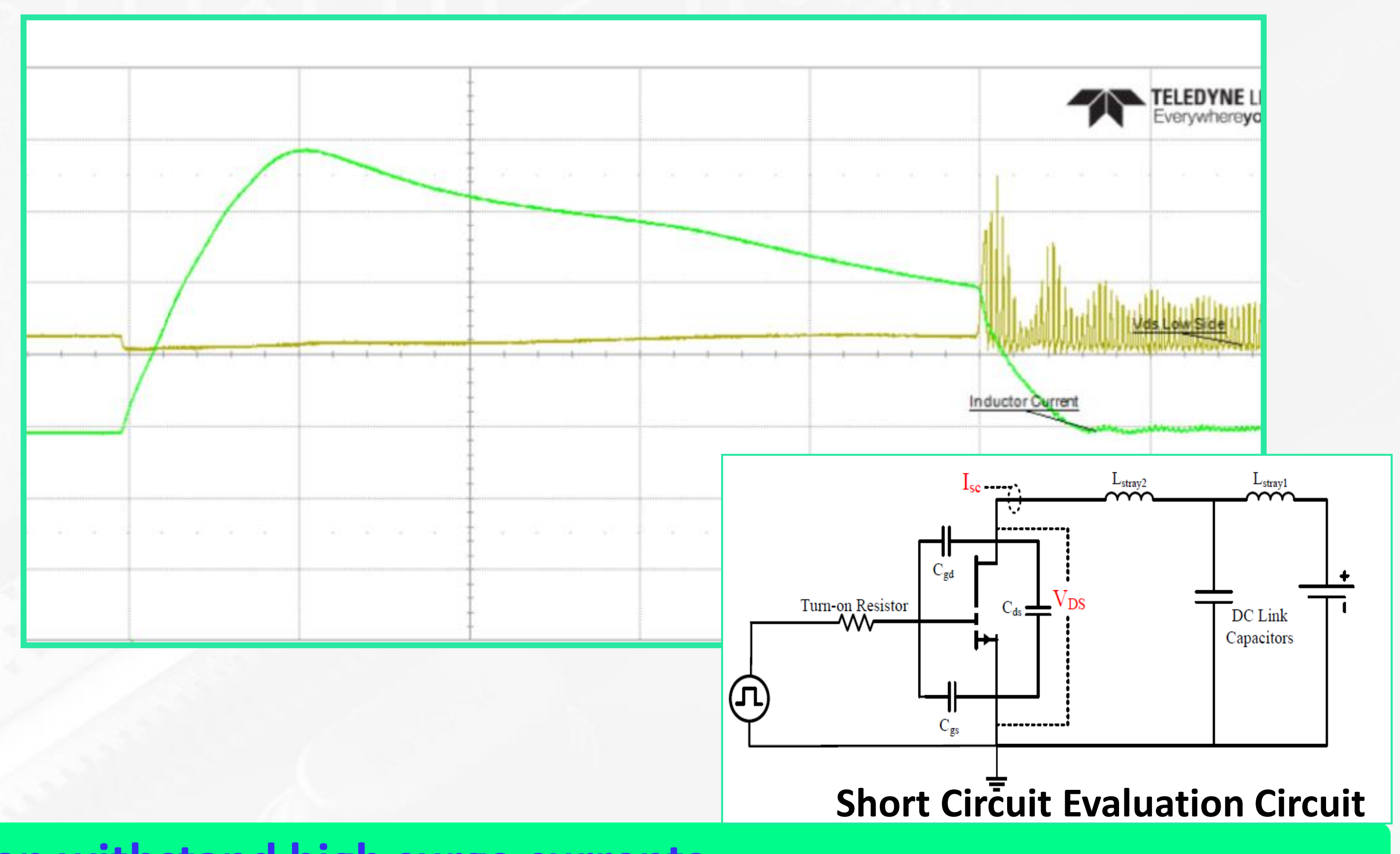
Initial Surge Current Capability Evaluation

- GaN devices do not operate in at or near the saturation region
- No internal limitation to device current during a short circuit event
- Proper current limiters are needed for safe operations
  - ‼ **See App note**
- Preliminary results for 80A rated device show operation of 395A for 5us
- Failures in standard surge current testing were result of voltage spike during turn off



Short Circuit Evaluation Circuit

D³GAN can withstand high surge currents

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Short Circuit Testing From AQG 324

- Two types of tests defined in AQG 324

Hard Switching Failure

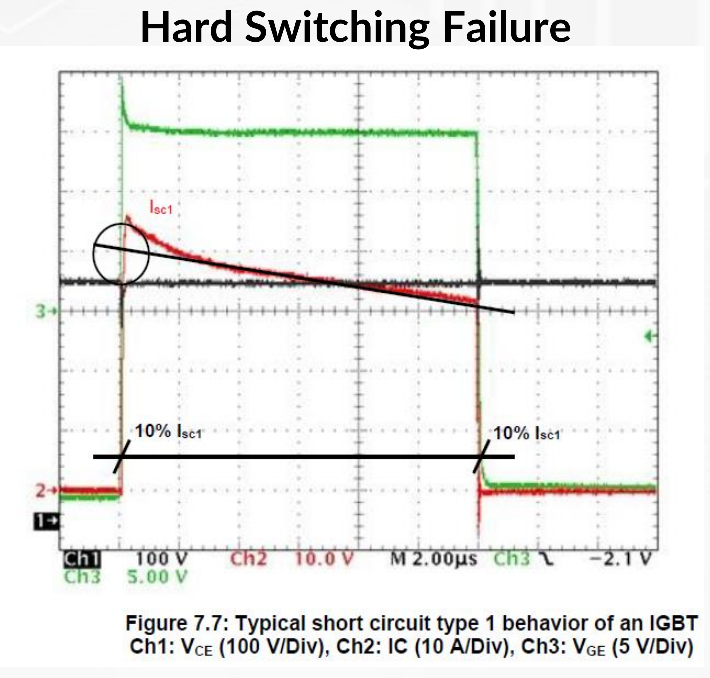

Figure 7.7: Typical short circuit type 1 behavior of an IGBT
Ch1: V_{CE} (100 V/Div), Ch2: IC (10 A/Div), Ch3: V_{GE} (5 V/Div)

Failure Under Load

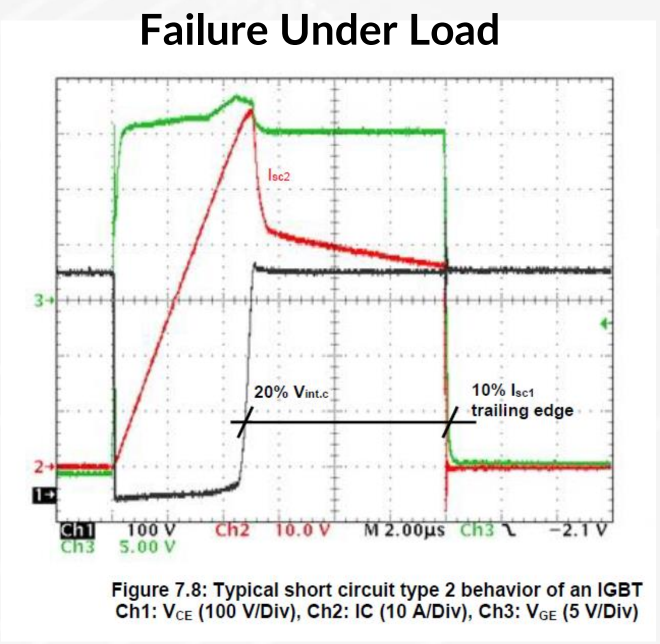

Figure 7.8: Typical short circuit type 2 behavior of an IGBT
Ch1: V_{CE} (100 V/Div), Ch2: IC (10 A/Div), Ch3: V_{GE} (5 V/Div)

- Both tests reference the saturation current (not applicable in lateral GaN)
  - Hard switching failure testing uses limited inductances to prevent reaching saturation
  - Failure under load must not desaturate within 5 usec

Current guidelines do not address the unique nature of lateral GaN

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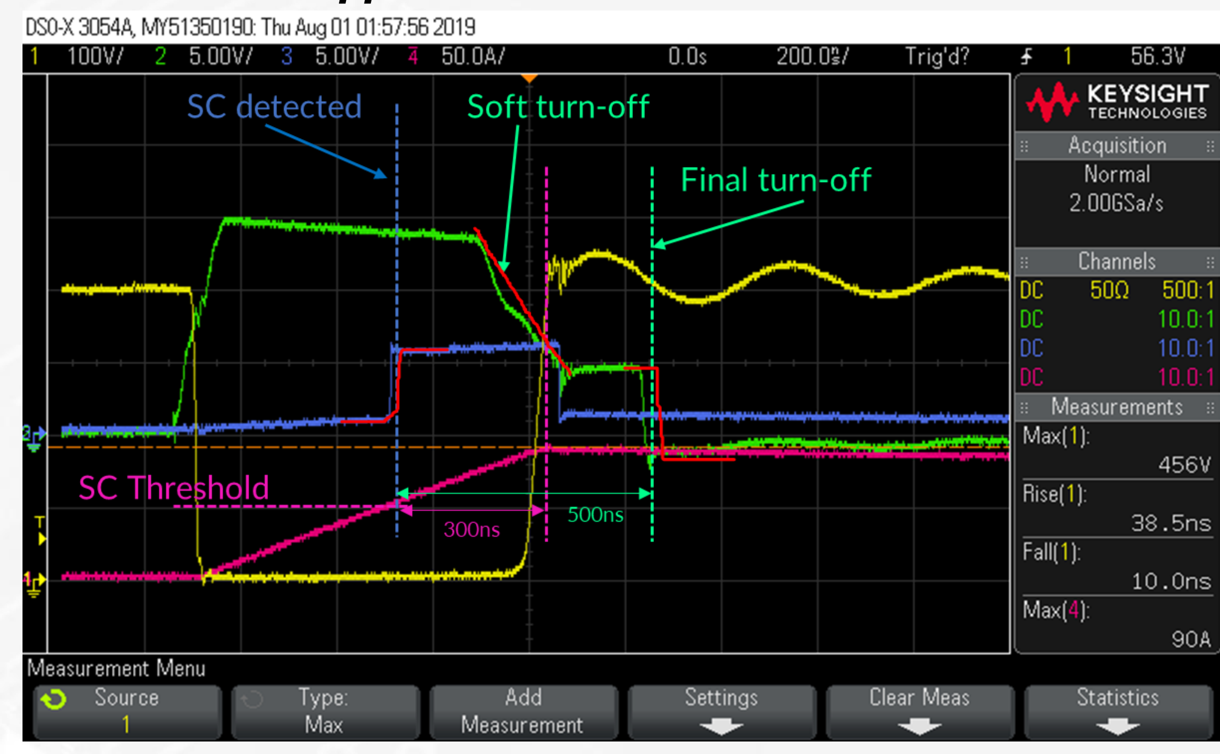
Surge Current Protection

- Commercial short circuit protection schemes do not protect GaN power devices
  - **Device heats up and fails @ 0.3 usec versus the 1 – 2 µsec of circuit response time**
  - **Circuits typically use saturation voltage sense to trigger**
- Developed circuit that will sense and turn off device more quickly
  - **Soft turn-off (1st stage) in < 0.3usec**
  - **Final turn-off (2nd stage) in 0.5 usec**
  - **Derivative circuit that triggers on rate of change and on current level**

SC Protection Application Note APN-01650-0003 Rev1.0



Yellow - Vds 100 V/div
Green - Vgate 5 V/div
Blue – comparator output 5V/div
Red – Coil current
Horizontal: 200 ns/div

2 stage turn off provides better protection

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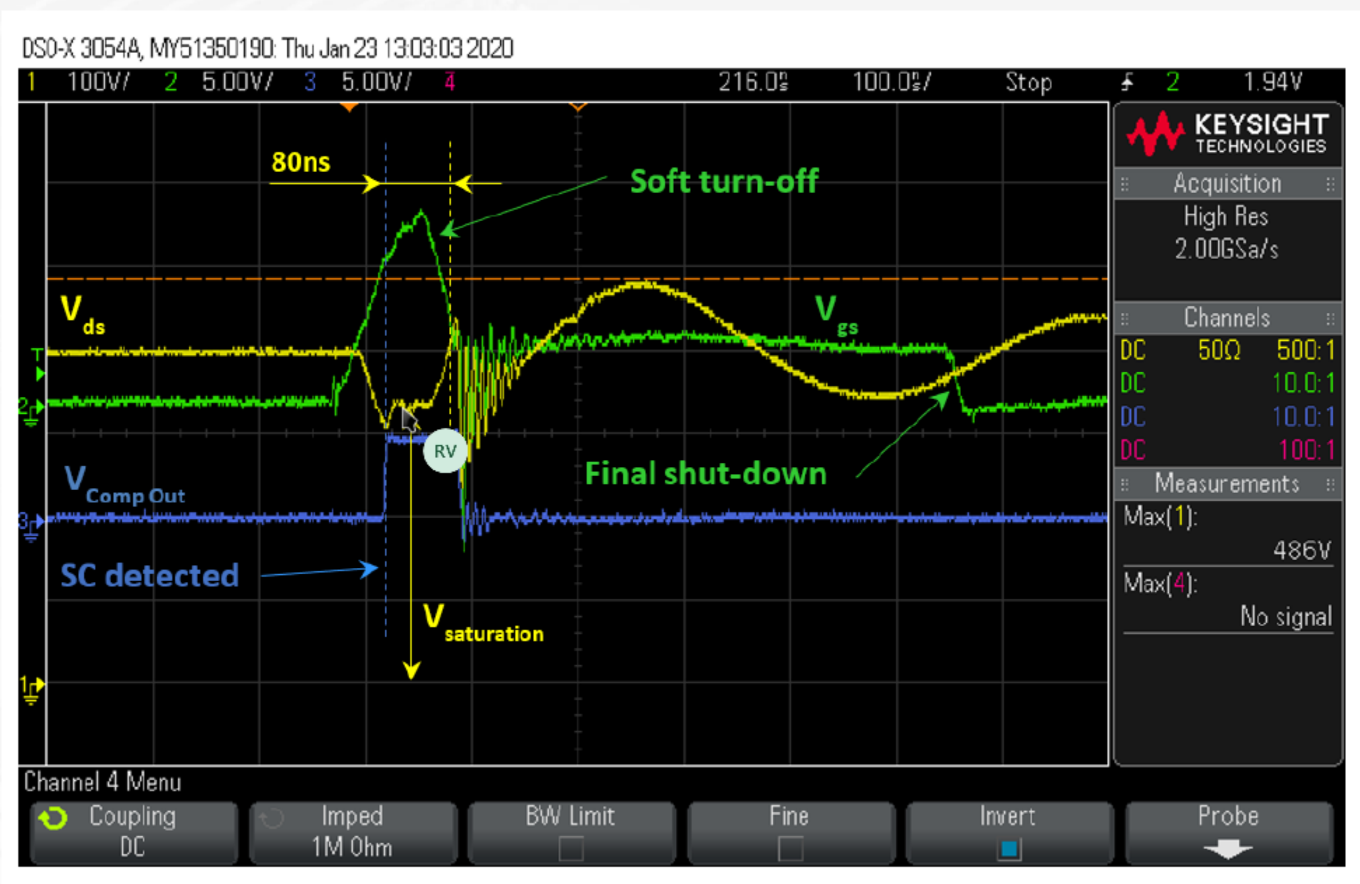
Over Current Protection

- Short circuit event has small drop in VD in GaN
- SC protection circuit senses the rapid change in current
  - Comparator circuit on Q2 (Silicon LV FET)
- Starts shutdown procedure within 80nsec
- Stage 2 shutdown within ~ 500 nsec



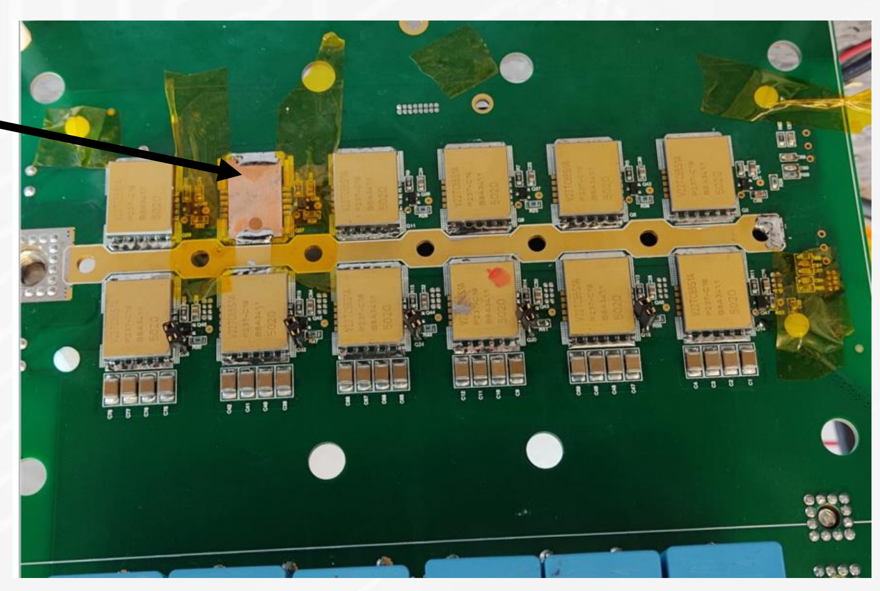
Over current protection begins in 80ns

SC Protection Circuit on Parallel Devices

- Parallel operation of devices allows device failures to influence all devices
- Demonstrated protection of SC on a single device does not necessarily correlate with devices in parallel
- VisIC SC protection method has been applied to a 6 pack board (12 devices in parallel)
  - Half bridge configuration

Parallel Device Surge Current Testing

Coil	Vin	Response time
3.2µH	400V	<500ns
0.55µH	400V	~200ns
2nH	300V	~100ns
2nH	400V	~100ns



- All conditions resulted in a controlled shutdown and no damage to any additional die

SC protection of D^3GAN has been demonstrated on parallel device

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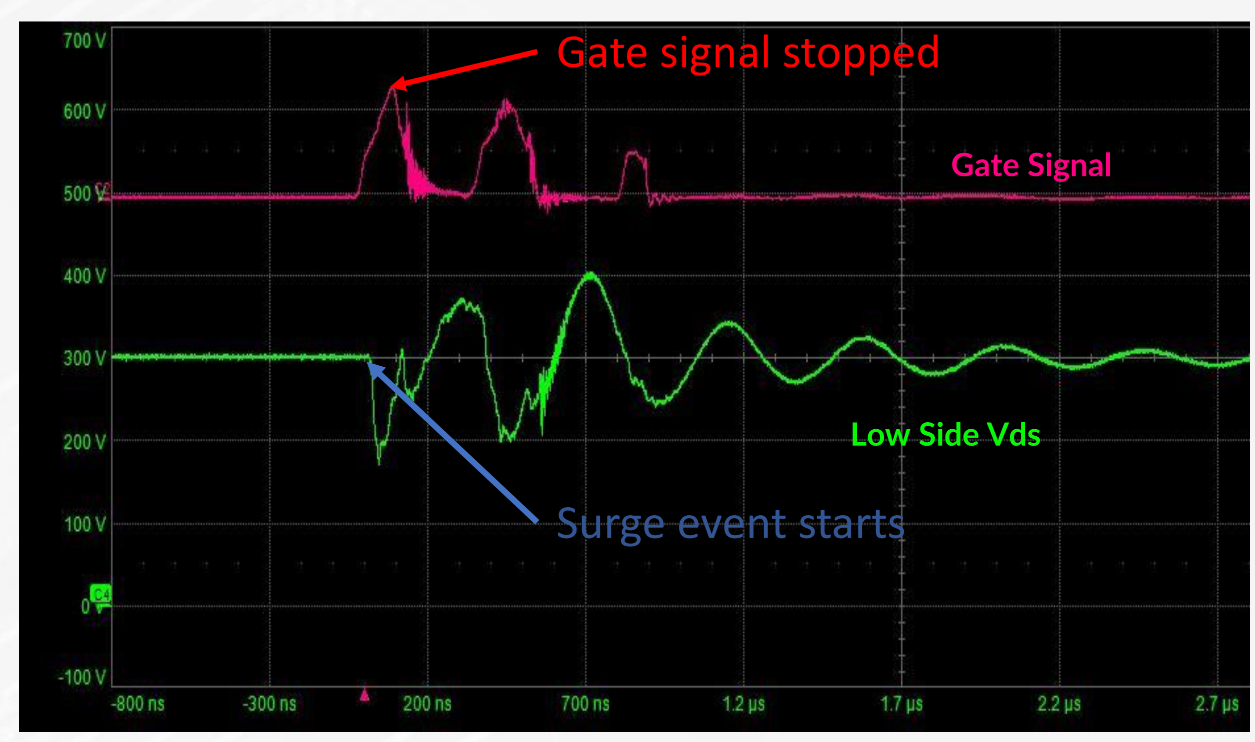
Surge Current Results for Parallel Devices

- Copper foil jumper used to simulate short circuit
  - 2nH inductance
- Input voltage = 300V
- Initiation of the shutdown procedure is ~ 100ns after surge even occurs
- Board verified to be fully functional after testing



Full protection of board has been demonstrated

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Case Study 400V 2L BEV Inverter

Tested at OEM with motor

3 phase, 400V, 500Apk, 350Arms, reaching

V Phase Current

U Phase Current

W Phase Current

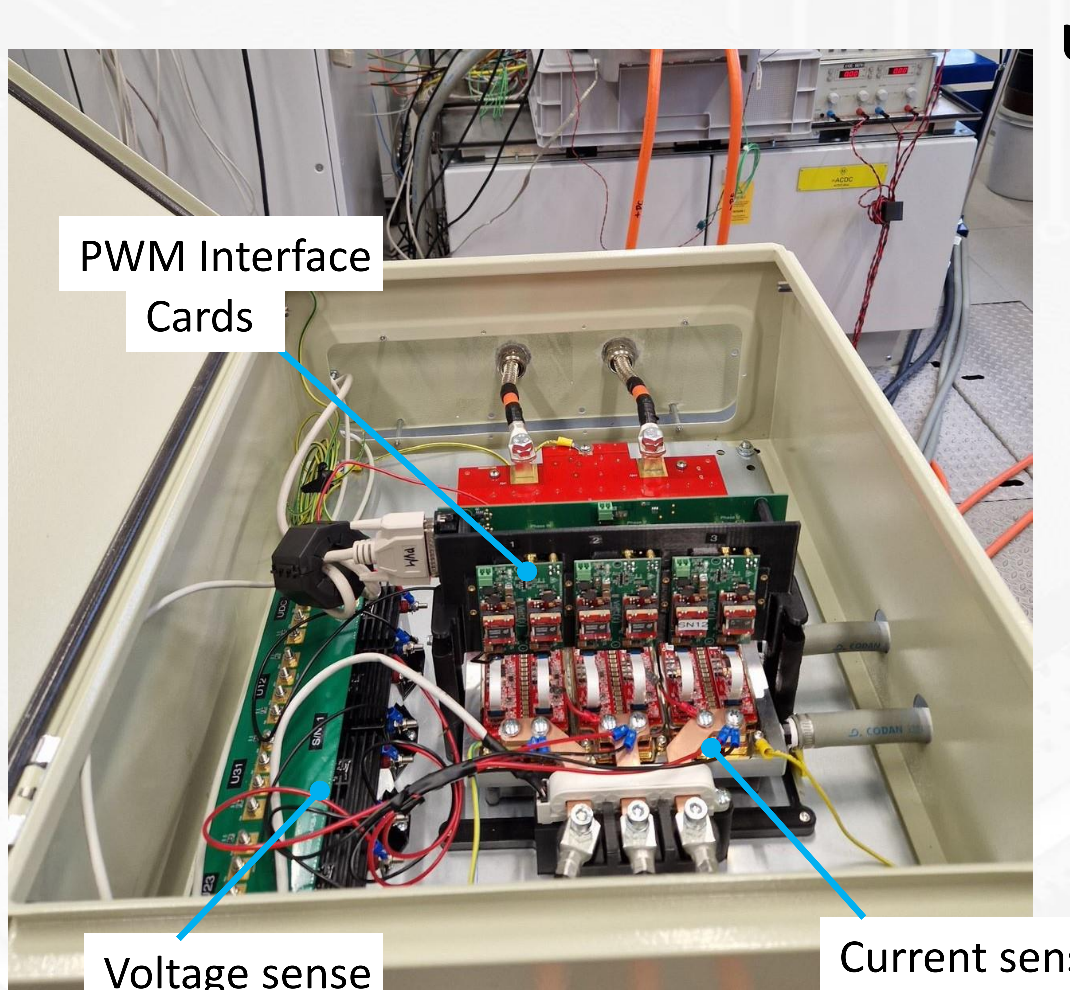
Meas	Type	Value
Meas 1	Top	μ': 512.1 A
Meas 2	RMS	μ': 367.7 A
Meas 3	Top	μ': 517.8 A
Meas 4	RMS	μ': 351.8 A
Meas 5	Top	μ': 449.4 A
Meas 6	RMS	μ': 348.6 A

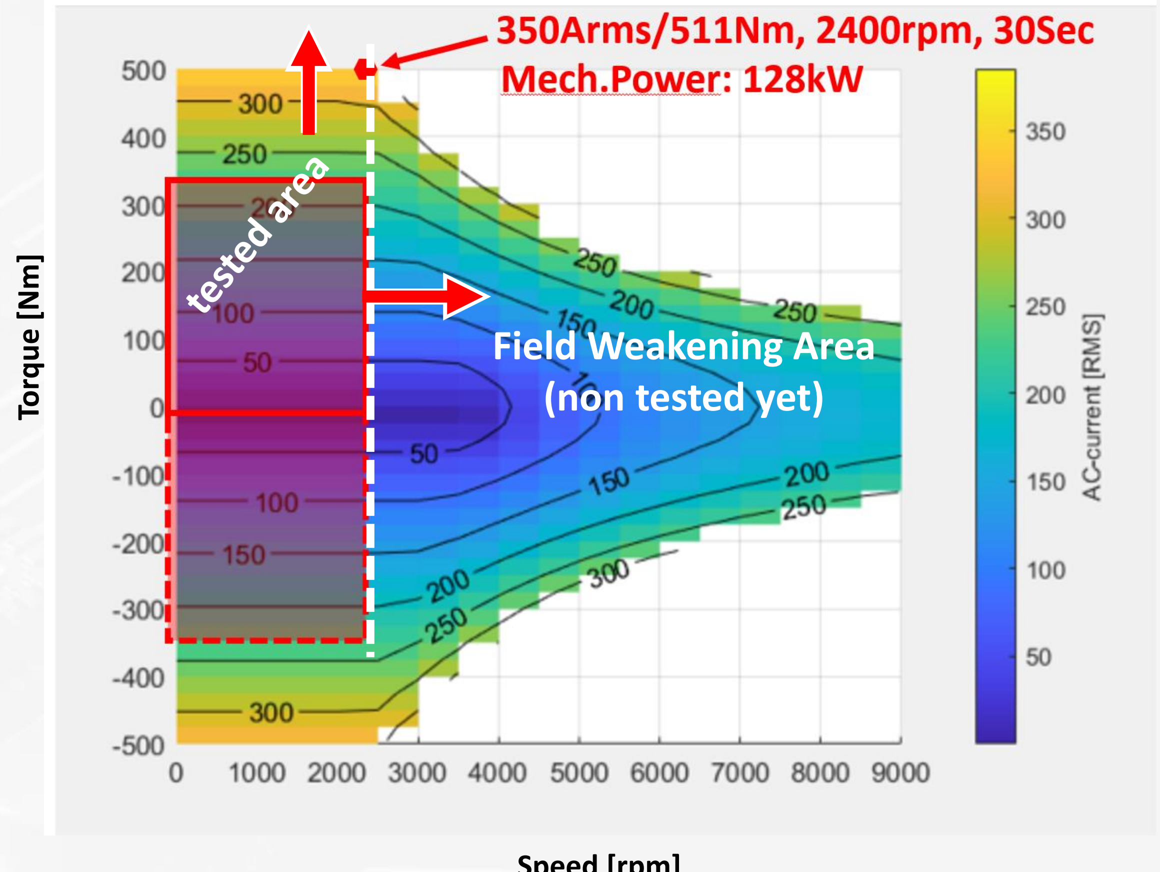
4 x 8 mOhm GaN die

2.2mΩ 650V HB D^{3}GaN Power Module (& Driver Module) Prototype, Based on VisIC V08 FETs

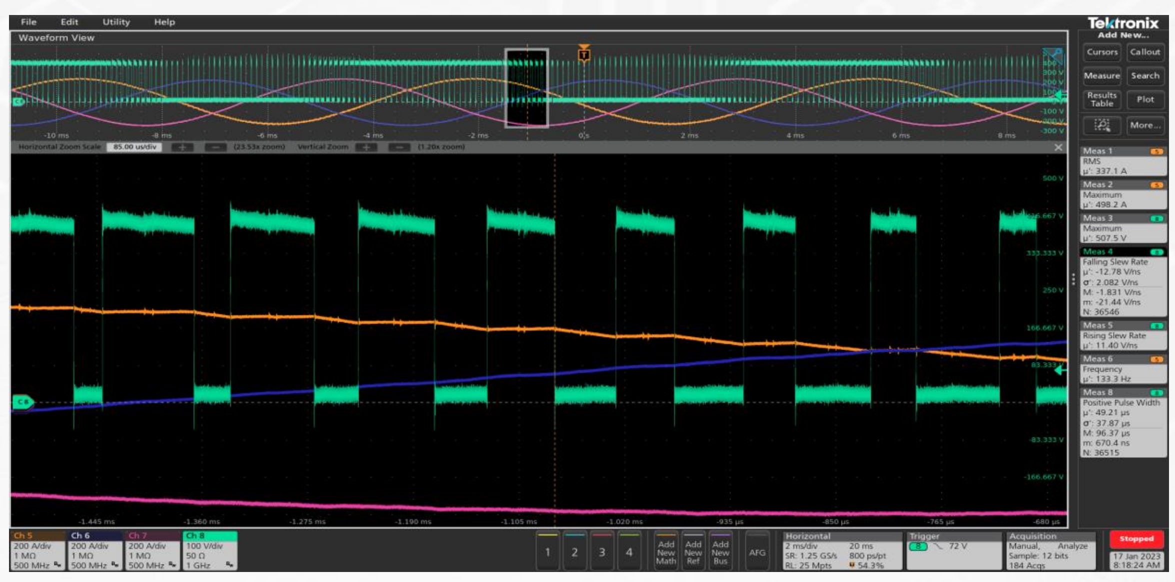
Results: 400V EV GaN based prototype

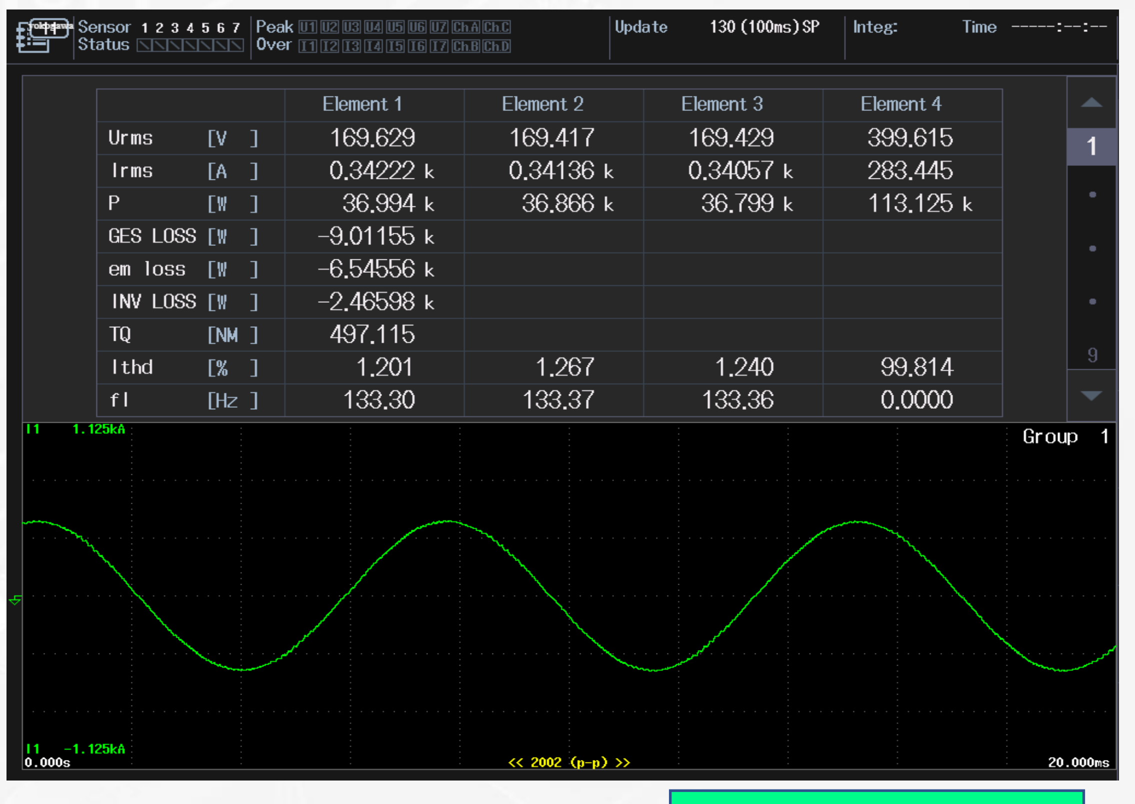
3-Phase GaN Inverter , Closed loop DYNO set up, tested up to 113 kW





High Power Operation Achieved
350Arms (500A peak) @400V for 30sec





		Element 1	Element 2	Element 3	Element 4
Urms	[V]	169.629	169.417	169.429	399.615
Irms	[A]	0.34222 k	0.34136 k	0.34057 k	283.445
P	[W]	36.994 k	36.866 k	36.799 k	113.125 k
GES LOSS	[W]	-9.01155 k			
em loss	[W]	-6.54556 k			
INV LOSS	[W]	-2.46598 k			
TQ	[NM]	497.115			
Ithd	[%]	1.201	1.267	1.240	99.814
fI	[Hz]	133.30	133.37	133.36	0.0000

2400 RPM

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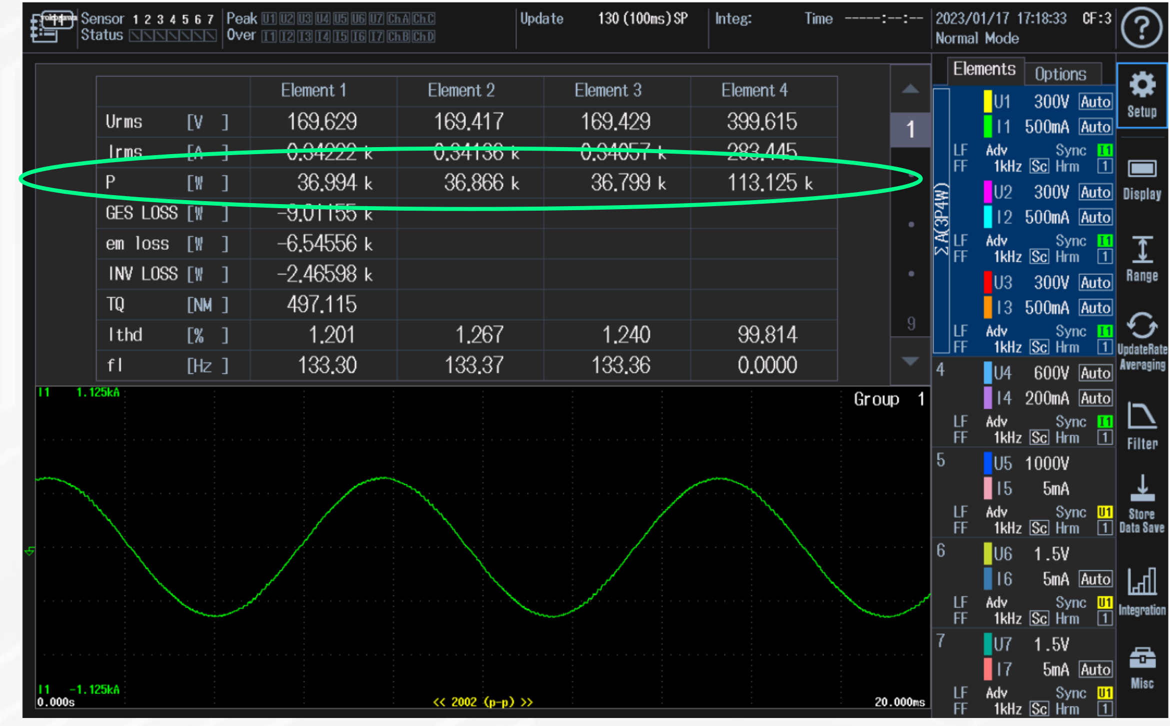
High Efficiency



400V 280ARMS 2000RPM 30sec - Efficiency 98.39% @10V/ns

400V 350ARMS 2000RPM 30sec - Efficiency 97.82% @10V/ns

WLTP Driving Cycle Efficiency

- ❑ Max Efficiency point:
  - ➢ **99.295%**
  - ➢ 2400RPM (160Hz)
  - ➢ 92.8NM
  - ➢ 24.4KW output

efficiency [%] vs. Torque [Nm]

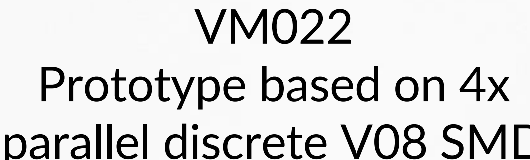
efficiency [%]: 90, 91, 92, 93, 94, 95, 96, 97, 98, 99, 100

Torque [Nm]: 0, 100, 200, 300

RPM
- 200 - 800
- 800 - 1200
- 1200 - 1800
- 1800 - 2200
- 2200 - 2400

Future Outlook

VisIC GaN Module Outlook



VM022
Prototype based on 4x parallel discrete V08 SMD

4.4mΩ 650V Half-Bridge D³GaN™ Power Module

VM044HB065WT1TM11X00

Description

The Transfer Molded Half Bridge module integrates 8mΩ Power FETs for a 300A$_{rms}$ class inverter and can be paralleled for higher power. The D³GaN™ technology uses high-density, lateral GaN power transistor, assembled into a Normally-Off product with extremely low $R_{DS(ON)}$ and exceptionally efficient switching performance.
The integrated safety functions ensure safe operation during system start up and shutdown, while having no impact on the switching performance of the GaN transistor.

Key Features

- Low inductance terminal connection to Busbars
- Weldable power terminals
- Thermal case designed for sintering to the heatsink
- High Threshold voltage for fast switching transients
- High performance SiN ceramic substrate
- Standard 15V gate drive voltage
- NTC sensor
- Package Size 50x38x6mm

Applications

- Hybrid and Electric Vehicle Traction Inverter
- High Power DC-DC Converter

Key Performance Parameters

Parameter	Value
V_{DS} (V)	650
$R_{DS(ON)}$ (mΩ)	4.4
Q_G (nC)	222
I_D (A)	360

VM044
2x V08/switch position
Sample Available Q3 2023

	VM044
Power Loop	5.7nH
Miller Current Gate Loop	3nH
Size	50x38x6mm

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Summary

Summary

- Today
  - D^3GaN reliable operation for high current BEV Inverter application
  - Proof of paralleling & short circuit detection methodology
- Future Works
  - Higher integration of Power Modules using 2nd Gen D3GaN chip for scalable inverter solutions
  - 3 Level NPC Inverter topologies to serve 800V BEV battery market

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THANK YOU