This application note provides recommendations for the driver design to properly operate VisIC's V22N65A* and V22S65A* ALL-Switch including control signal sequencing and considerations for PCB layout.

ALL-Switch contains a GaN power transistor using a patented high-density lateral layout. The resulting product has extremely low $R_{DS(on)}$, exceptionally fast switching performance and a small package footprint. It is effective in applications requiring high efficiency and low cost to implement high power-density designs.

Overview of ALL-Switch Operation

ALL-Switch is a System In Package (SIP) power switch. It is built as a multi-chip module. ALL-Switch operates as a safe, normally-OFF device through its SmartGaN topology, an innovation by VisIC Technologies. In comparison to common cascode-connected devices, where a low voltage, normally-OFF silicon MOSFET is modulated by a switch driver to indirectly control a GaN transistor; the ALL-Switch design is based on directly modulating the high voltage GaN transistor. The normally-OFF silicon MOSFET in ALL-Switch is turned on while ALL-Switch is sequenced on and then held in continuous conduction (short mode) during normal operation. This method of design and operation eliminates parasitic effects like the silicon MOSFET body diode's reverse recovery.

SmartGaN design also provides an exceptionally low voltage drop during reverse conduction mode by minimizing the resistance. The lack of minority carriers in both forward and reverse current conduction realizes zero recovery time.

The internal design of ALL-Switch insures safe operation in the case of driver fault, power supply failure, or improper *turn on/turn off* both Vaux and HV bus.

The threshold voltage of the GaN transistor exceeds 5V, thereby ensuring high EMI immunity in harsh electromagnetic environments.

A SiC diode in parallel with the GaN transistor in V22S65A, provides a very low voltage drop in reverse conductivity mode when ALL-Switch is used to switch inductive loads.

*There are two versions of devices:
V22N65A – without parallel sic diode
V22S65A – with parallel sic diode

Simplified All-Switch Control Block Diagram

Figure 1 is a simplified block diagram of ALL-Switch control circuit.

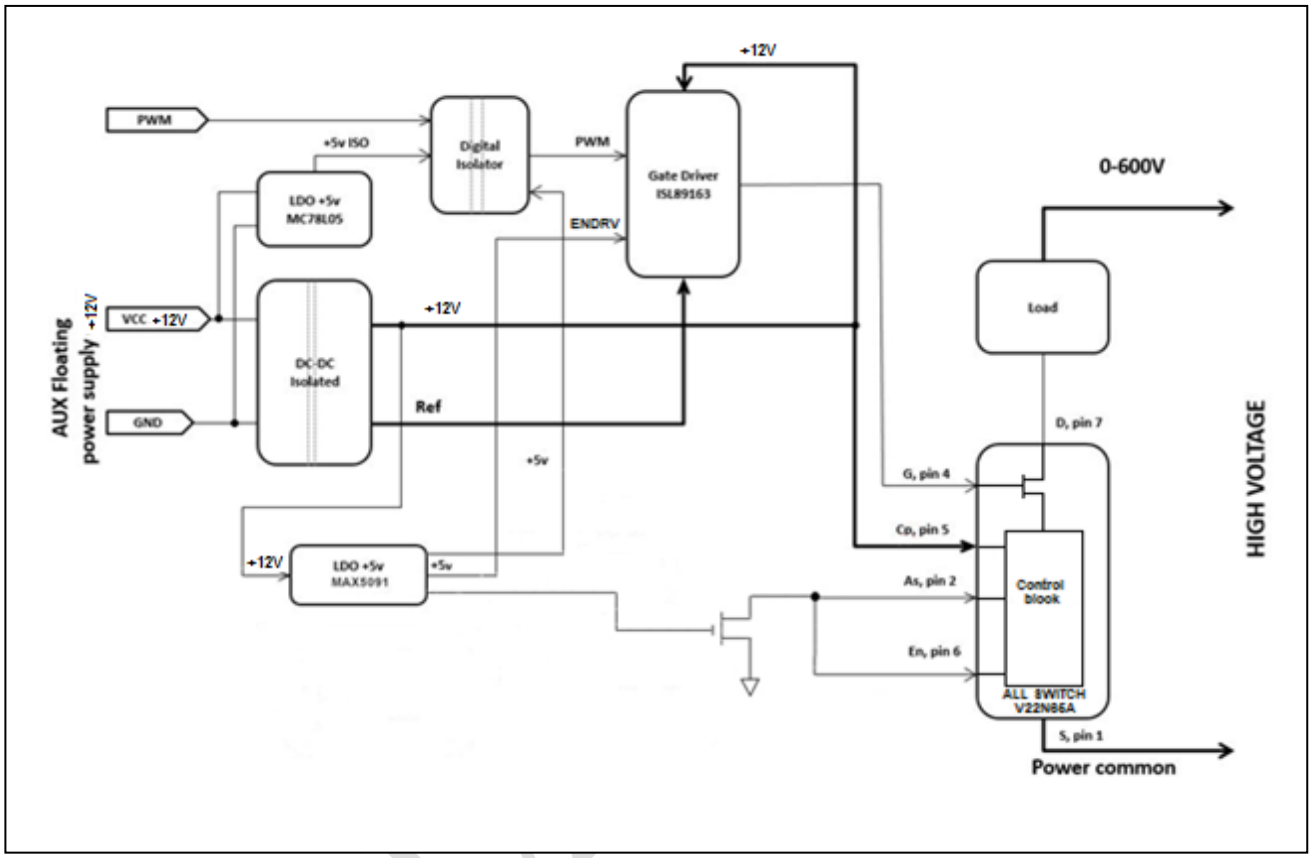


Figure 1 - ALL-Switch Control Circuit Block Diagram

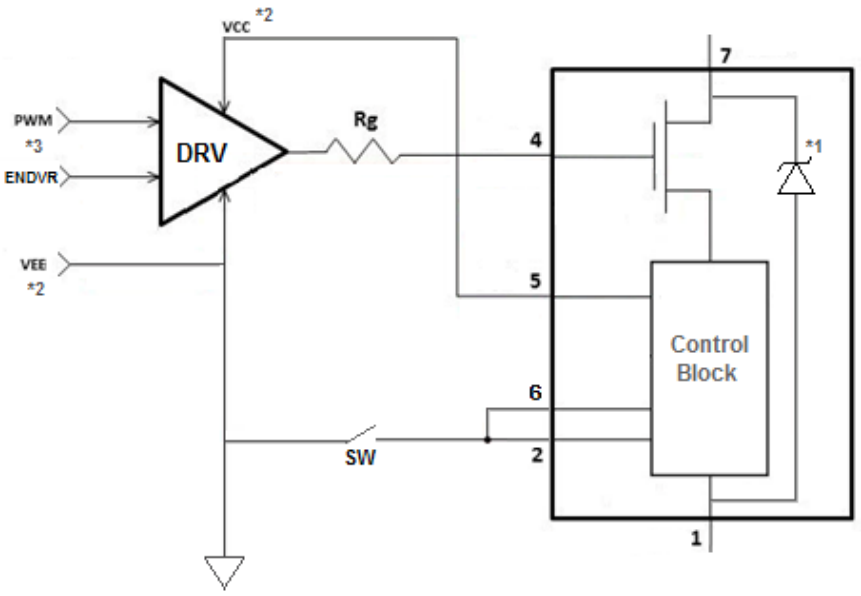


Figure 2 – Activating the Control Block

Control block (pins 2,6) gets -12V activating voltage refer to pin 5.

The SW activated by MAX5091 in our case.

*1) Optional SIC Diode for V22S65A

*2) VEE -12V to VCC
VEE/VCC – Aux 12V

*3) PWM & ENDRV – Logic level (TTL or CMOS)

System Power Up Operation

The system's Aux power up timing diagram is depicted in Figure 3. After the auxiliary power supply turns-on and all required voltages have stabilized, the Power Supervisor IC provides enable signal SW.

After this sequence ALL-Switch is functional and ready to be driven by PWM inputs to the gate driver.

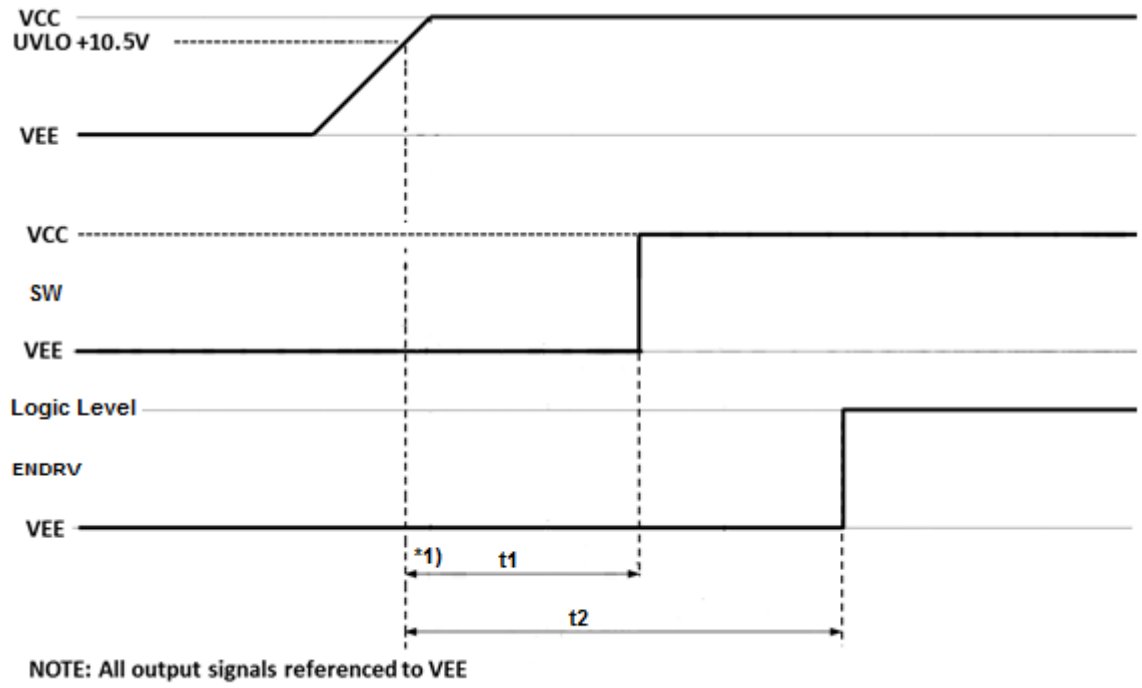


Figure 3 - System Power Up Timing Diagram

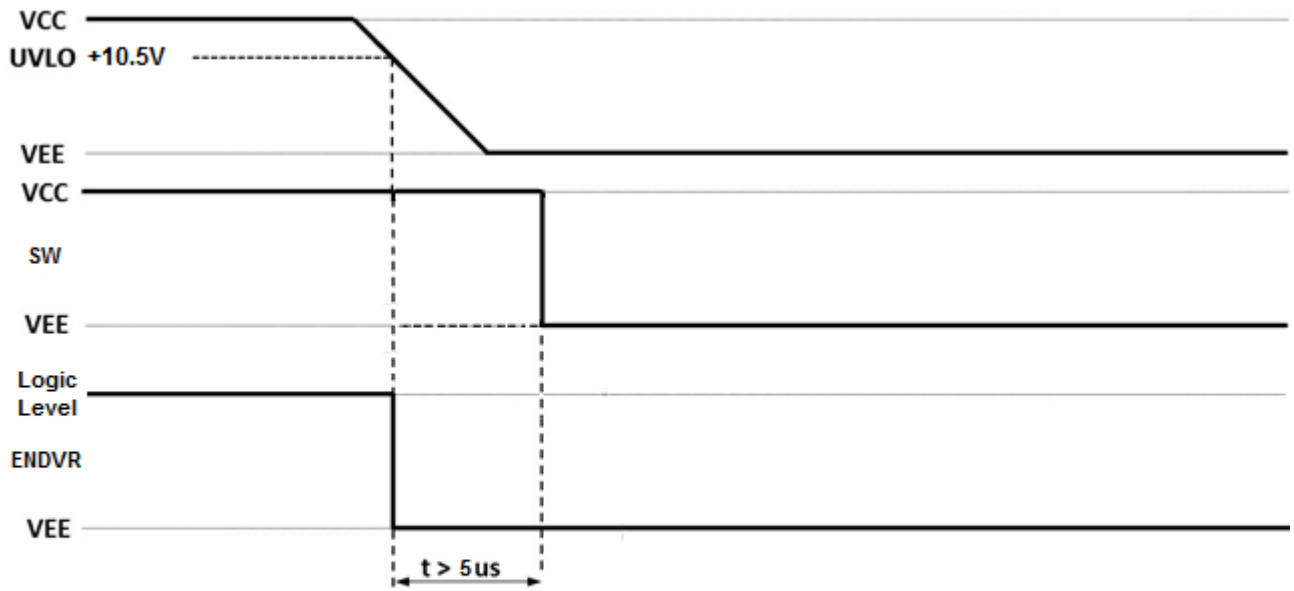
*1) Time delay t1 is approximately 5µS, but has to be less then t2.

System Power Down Operation

Normal System Power Down

The system's power down timing diagram is depicted in Figure 4.

When the auxiliary power supply voltage drops below the UVLO level (10.5V) the power supervisor activates SW. ENDRV disables the gate driver.



NOTE: All output signals referenced to VEE

Figure 4 - Normal Power Down Timing

Application Guidelines

Layout and Interconnection Guidelines

Figure 5 shows the current path when the gate driver turns the ALL-Switch device on. Ideally, the driver provides the current flow directly from the gate to the source of GaN transistor via small circuit loop. For the shortest turn-on time the resistance and inductance in this path must be minimized.

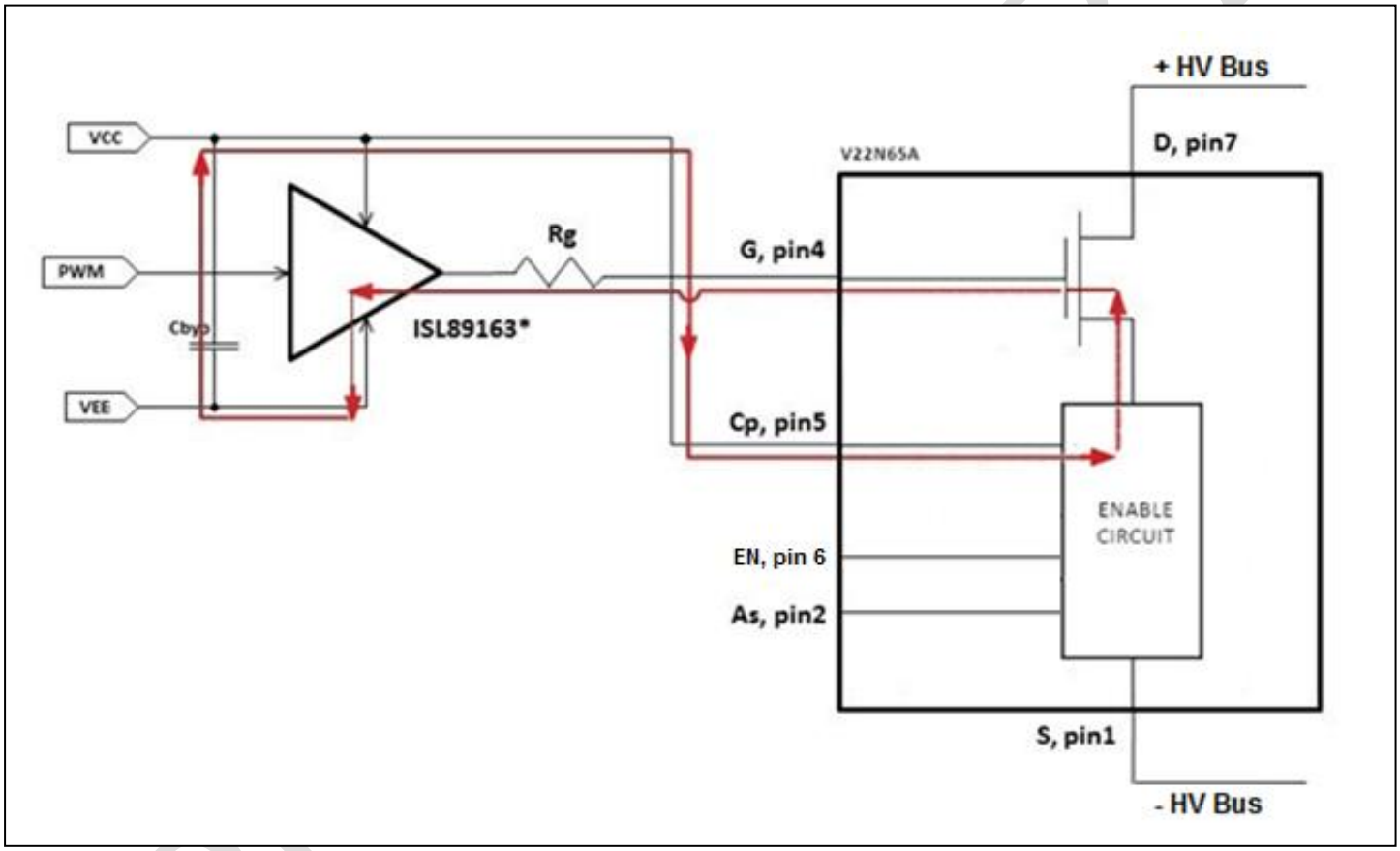


Figure 5 - Drive Current Path

* Customer can use any other appropriate driver

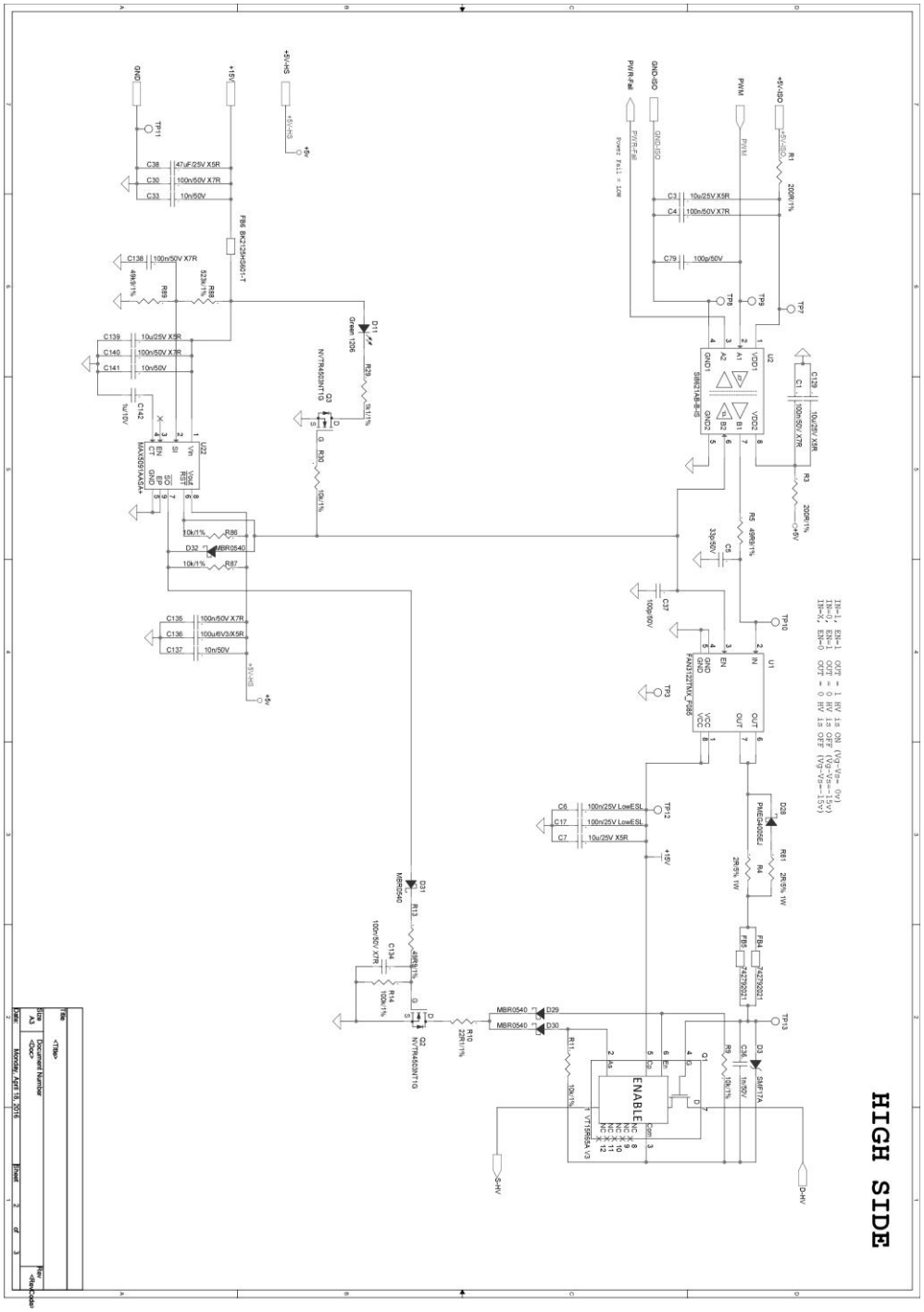
Cbyp should have low ESR and ESL. Its placement and value are provided in the driver's datasheet.

The driver used in this application note incorporates fast input circuits, short propagation delays and output stages able to deliver over 6A peak current with transient times from 2ns to 15ns. The layout and connection recommendations that should be followed to achieve peak performance are:

- Keep high current output and power ground paths separated from logic input signals.
- Keep the driver as close to the transistor gate as possible to minimize the length of traces.
- For best results, make connections to all pins as short, wide, and direct as possible.
- The turn on and turn off path lengths should be minimized and have low inductance. VisIC recommends using a 4-layer PCB to reduce trace inductance. Detailed recommendations are provided in driver IC application notes.

Appendix A

The electrical circuit of the ALL-Switch driver stage is shown below.



Any other appropriate driver; e.g., FAN3122TMX driver, may be used.